PETsys Electronics
Medical PET Detectors S.A.

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PETsys Electronics

PETsys SiPM Readout System

§ 1. Introduction.

The PETsys SiPM readout system is designed for reading a large number of SiPM photo-sensor pixels in applications where a high data rate and excellent time resolution is required. The readout was developed with the application in Time of flight PET in mind, but it can also be used in many other applications where one needs to read a large number of SiPM pixels. The readout is based on the TOFPET2 ASIC [1]. This is a low power ASIC with 64 channels optimized for reading SiPMs for Time Of Flight PET applications. The ASIC is the interface between the analog signals from the photo-sensors and the digital readout. Every time one of the 64 channels in the ASIC exceeds the configurable set of thresholds, an event record is created giving the channel number, the time and the charge of the event. The rest of the readout chain only handles digital data. The system is typically equipped with PETsys TOFPET 2C ASICs , but can also be equipped with PETsys TOFPET 2D ASICs. This ASIC can be configured to read either positive or negative signals. This allows the readout to be used for with Micro Channel Plate PMTs and similar sensors producing negative pulses.

The readout system has four main components: the Front-End module, the Front-End type D unit, the Clock&Trigger unit and DAQ unit. Together these boards allow assembling a complete and scalable data acquisition system reading tens of thousands of independent SiPM pixels.

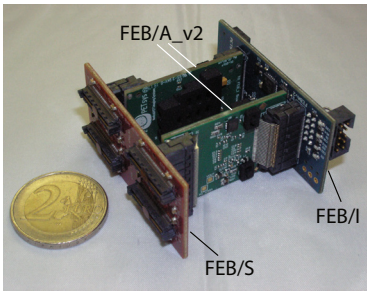

Figure 1. FEM128
The Front-End Module FEM128 has two ASICs and reads 128 SiPM channels. It measures 25.4x53.1x54.0 mm.

§ 2. The PETsys Front-End modules.

The PETsys Front-End Module is the front-end readout module for reading SiPM arrays, or micro-channel plate photo-detectors. It is the interface between the analog signals of the photo-sensor and the digital readout chain. After the font-end module only digital signals are used. The front-end module may have to be adapted to the particular application. But we have 2 “standard”: front end modules: the FEM128 and the FEM256. These are described below.

The Front-End Module version FEM128 (Fig. 1) has 128 channels. It is optimized for systems requiring a high channel data rate. The Front-End Module is made-up from three different boards: FEB/A_V2, FEB/S and FEB/I. This allows for easy customization for different SiPM types and scanner geometries. The FEM128 has two FEB/A_V2 boards (Fig. 2). Each FEB/A board has one PETsys TOFPET2 ASIC with 64 channels. These boards are mounted perpendicular to the SiPM arrays, and this geometry allows to control and stabilize the temperature of the SiPM array. The board also has a temperature sensor near the ASIC.

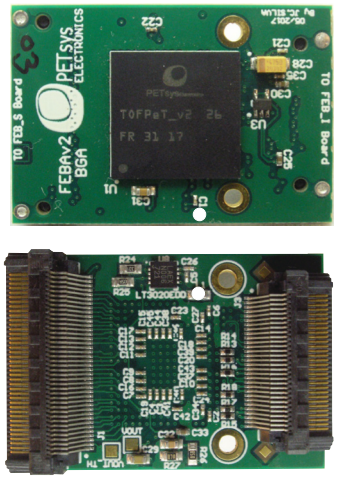

Fig. 2: FEB/A_V2
Top and bottom view. The connector to the right connects to the FEB/S, the connector to the left connects to theFEB/I . The board, including connectors, measures 39x25 mm.

The FEB/S board is a purely passive board adapting the SiPM array to the input connector on FEB/A_v2 board .This board will be different for different SiPM array models. The version of the FEB/S board shown on figure 1 has two pairs of connectors that directly take the following Hamamatsu MPPC arrays: S13361-3050AS-08, S13361-3075AE-08 and S14161-3050AS-08. Each FEB/S measures 53.1 x 25.4 mm and is four-side buttable such as to allow forming a continuously sensitive area with almost no dead space. The FEB/S also has two temperature sensors, each located in the middle between the pair of connectors taking one SiPM array.

Fig. 3: SAMTEC HQCD cable.
A flat coax cable assembly connects the Front-End Module to the PETsys FEB/D unit. The standard length is 50 cm, buy this cable can be up to 300cm

The FEB/I allows the FEM128 to communicate with the FEB/D. It is equipped with a MAX 10 Altera FPGA and adapts the electrical communication protocol from LVCMOS in FEB/D to LVDS in the ASIC and reads the analog temperature sensors in the FEM128. Up to eight FEM128 modules can be connected to one FEB/D-1k unit using a SAMTEC HQDC-030-xx.00-TTL-SBL-1N flat cable (Fig. 3). This cable can be up to 300 cm long. It is also possible to plug the front-end modules directly into the FEB/D-1k unit.

The power dissipation of the ASIC is 8.6 mW/channel for the recommended settings. This power dissipation can be reduced to 4 mW/channel by using different settings, but this results in a slight degradation of the timing performance. The LVDS buffers and LDO voltage regulators of the FEM add 6mW/channel and bring the total power consumption of the FEM at 14.6 mW/channel.

[1] Experimental characterization of the TOPET2 ASIC, R. Bugalho et al., JINST_079P_0918
See our web site under documentation for the data sheet of the ASIC

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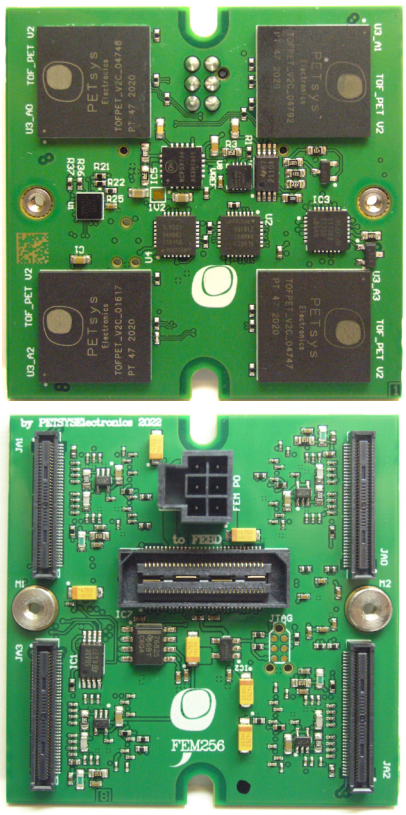

Figure 4. PETsys FEM/256 board.
Figure showing the two sides of the FEM256 board.

Figure 5. PETsys FEM/256 detector module.
This figure illustrates how to build a detector module based on the FEM256 board. The cooling solution must be adapted to the particular scanner geometry. .

In the FEM128 the data output of the ASIC uses 4 LVDS data lines at up to 800 Mbps per data line. The events are encoded in 80 bits. The maximum event rate between the FEM128 module and the FEB/D unit is about 500 kcps per channel.

The FEM256 module is optimized for large systems and lower per channel cost, it allows more compact PET detector modules, and makes the design of the cooling easier.

The board is shown on figure 4. In this front-end board the functionality of the FEB/A and FEB/I of the FEM128 are implemented in one single board. The board is also equipped with a MAX 10 Altera FPGA and adapts the electrical communication protocol from LVCMOS in FEB/D unit to LVDS in the ASIC and reads the analog temperature sensors. The board measures 50x50 mm^2 and connects to the FEB/D unit using the same SAMTEC HQC cable (Fig 3). In the FEM256, each ASIC used two LVDS data lines at up to 800 Mbps per data line to output the data. This limits the maximum count rate per channel to 300 kcps.

The FEM256 module can connect to the FEB/D-1k unit , or the FEB/D-8k unit, using the board using the same SAMTEC HQDC-030-xx.00-TTL-SBL-1N flat cable (Fig. 3)

Figure 5 illustrates how the FEM256 can be integrated with the mechanics and cooling. An aluminum cooling bar is inserted between the FEM256 board(top) and the FEB/S-256 board(bottom) with the SiPM arrays. The SiPM arrays are either reflow soldered on the FEB/S-256, or one uses a FEB/S with connectors. The ASICs in the FEM256 are directly in contact with the cooling bar. The cooling bar serves both for the cooling and for positioning the SiPM arrays. The FEB/S-256 measure 52x52 mm^2. Flex cables bring the signals form the SiPM arrays to the ASIC. This figure is only to illustrate the concept. The front end module will probably have to be adapted for the specific scanner design

Comparison FEM128/FEM256	FEM128	FEM256
# ASICs	2	4
# Channels	128	256
Power/ Channel	14.6	14.6
# Temperature sensors	2+2	4+4
Data rate link (Mbits/s)	800	800
# Links per ASIC	4	2
Event rate / channel (kcps)	500	300

§ 3. The PETsys Front-End type D unit.

The front-end FEB/D unit collects event records form the ASICs in the FEM modules and send these to the DAQ unit in the DAQ computer as assembled data frames. We have two versions of PETsys Front-End type D unit. The FEB/D-1k unit is optimized for small or medium system with up to maximum 16’384 channels, the FEB/D-8k unit is optimized for larger systems.

Synchronous readout of multiple FEB/D units is made possible by a connection to the Clock&trigger unit through a ERNI SMC connector carrying LVDS signals at 400 Mbit/s. This interface also provides for a trigger system allowing to discard events records that are not part of a coincidence. Such events records are not transmitted to DAQ unit. The FEB/D unit can also accept a veto signal from the Clock&Trigger unit.

The FEB/D units provides clock synchronization signals to the ASICs and receives configuration signals from the DAQ unit and distributes these to the ASICs. It receives the system clock (200 MHz), and synchronization and trigger signals from the Clock&Trigger unit. Both FEB/D units come with the same communication mezzanine. This communication mezzanine has two of SFP+ connectors for data output to the DAQ and for receiving the configuration signals. The SFP+ ports can either drive a optical cable or an SFP+ Copper cable.

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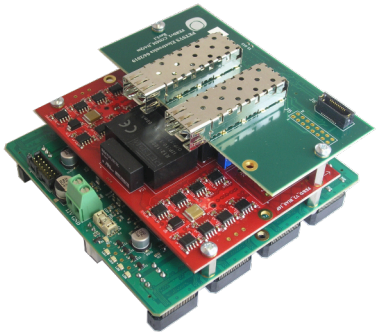

Figure 6: FEB/D-1k unit.
Top view of the FEB/D-1k unit showing the bias voltage mezzanine (red) and the SFP+ communication mezzanine (green) on top of it..

The second SFP+ port allows the FEB/D units to be daisy chained. One chain of FEB/D1k boards can have up to 32 boards. The SFP+ ports operate at 6.6 Gbit/s allowing a maximum event output rate of 100 Mcps for one FEB/D chain. It is also possible to connect both SFP+ ports on the same FEB/D to the DAQ unit; in this way the maximum data rate to the DAQ unit can be 200 Mcps.

A Gbit Ethernet communication mezzanine is also available for use with small systems. When using the Gbit Ethernet communication mezzanine the maximum data output rate to the computer is limited to 15 Mcps.

The FEB/D units are standard provided with latest version of the software installed.

The FEB/D-1k unit.

The front end type FEB/D-1k unit is shown on figures 6 and 7. It is composed of a FEB/D motherboard with a Kintex-7 FPGA_XC7K160T, a communication mezzanine, and a bias voltage mezzanine. Each FEB/D-1k mother board measures 104.5x104.5 mm. Power DC-DC converters and regulators on the FEB/D motherboard provide the low voltages (1.35 V and 3.2 V) for the ASICs in FEM modules.

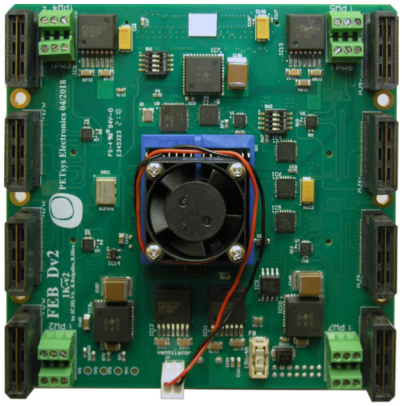

Figure 7.
Bottom side of the FEB/D-1k mother board showing the 8 connectors receiving the cables from the FEM128 modules.

Eight front-end modules FEM128 can be connected to one FEB/D-1k unit, using either direct board-to-board connectors or using flexible coaxial flat Samtec cables (Fig. 3). The FEB/D-1k unit can receive data from up to 4 FEM256 when using the low voltage power for the ASIC provided by the FEB/D-1k mother board. It can receive data form 8 FEM256 if the power to the ASICs on the FEM256 is supplied form external power supplies.

The middle mezzanine (the red board on figure 6) supplies bias voltages to the SiPMs. The de default mezzanine provides 16 positive bias voltages in the range 0-72 V, with a maximum current of 2.5mA per bias line. We can also provide a version providing a maximum current of 8.75 mA per line. We also can provide a bias voltage mezzanine with 64 bias voltage lines, same voltage range, 8 per FEM128. In this bias voltage mezzanine the maximum current is 550mA per bias line.

It is also possible to connect an external power supply for providing the bias voltage.

Main features of the FEB/D-1k unit:

- Reading up to 1’024 independent SiPM channels from 8 FEM128.
- Equipped with Kintex-7 (xc7k160t) FPGA .
- Comes with pre-installed firmware.
- Connects to up to eight Front-End Modules with 128 channels.
- Max output rate 6.6 Gbps, or 100 M events/s.
- Up to 32 FEB/D-1k units can be Daisy chained and connected to a single DAQ unit input.
- Clock frequency 200 MHz.
- External supply voltage: 12 Vdc, maximum 4 A.
- On board DC-DC converters supply power to the ASICs in the FEM boards.
- SiPM bias voltages produced in a mezzanine. The default mezzanine provides 16 lines, 5-100 V, positive, 3-9 mA per bias line.

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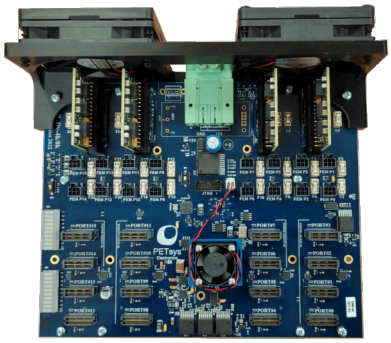

Figure 8
Top view of the FEB/D-8k mother board

The FEB/D-8k unit.

Each FEB/D-8k unit can control up to 16 of any of the front end modules, either FEM128 or FEM256. The FEB/D-8k is equipped with Kintex-7 and Spartan-7 FPGAs. Each FEB/D_8k board (Fig. 8 and 9) consists of a motherboard, measuring 208x166.3 mm2, and three mezzanine boards on the bottom side of it. The green middle mezzanine is the communication mezzanine. It is the same and on the FEm128, and provides the link to the DAQ unit in the DAQ computer. The two red mezzanine board provides 32 positive bias voltages in the range 0~60 V, and an average current per bias line of 2 mA (5 mA option on request). Optionally, we can also equip the FEB/D-8k with two times the same bias mezzanine (BIAS-16P) as the FEB/D-1k.

The FEB/D_8k unit needs to be supplied with 12 Vdc, maximum 25 A. The current depends on the type and number of FEM connected to it. Four DC-DC converters (visible on the top side of the mother board) and regulators provide power to the ASICs.

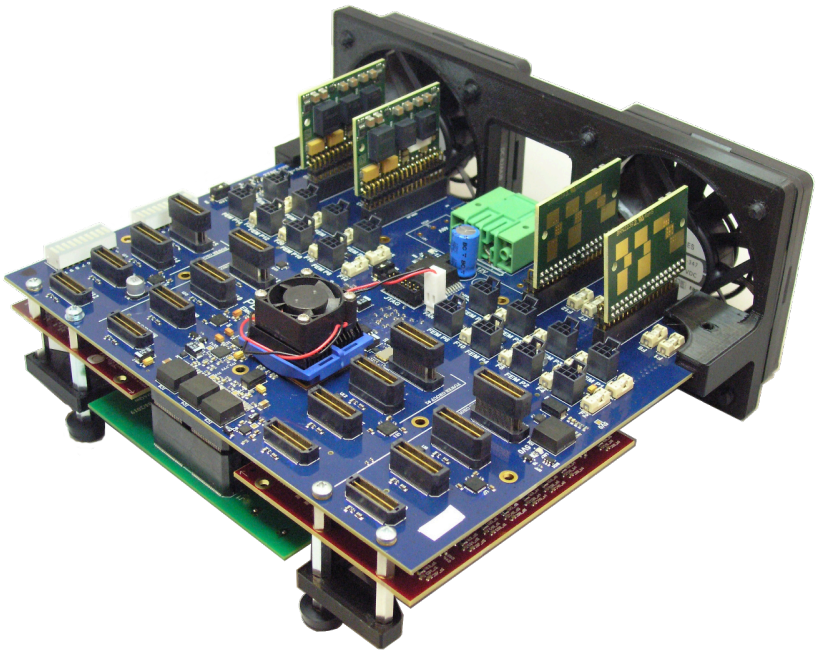

Figure 9. PETsys FEB/D-8k unit.
On the top side of the mother board there are four 4 DC-DC converters providing power to the ASIC and 16 connectors for the FEM modules. Under the mother board there are two bias mezzanines and one communication mezzanine

Main features of the FEB/D-8k unit :

- Reading up to 4’096 independent SiPM channels from 16 FEM modules.
- Equipped Kintex-7 (xc7k160t) and Spartan 7(xc7s50) FPGA .
- Comes with pre-installed firmware.
- Connects to up to 16 Front-End Modules either FEM128 or FEM256.
- Max output rate using one SPF+ link: 6.6 Gbps, or 100 M events/s.
- Up to 32 FEB/D-8k units can be Daisy chained and connected to a single DAQ unit input.
- Clock frequency 200 MHz.
- External supply voltage: 12 Vdc, maximum 25 A.
- On board DC-DC converters supply power to the ASICs in the FEM boards.
- SiPM bias voltages produced by two mezzanine boards. The default mezzanine type provides 32 biasing lines, independently configurable to 0-60 V, and able to supply 2 mA per bias line on average.

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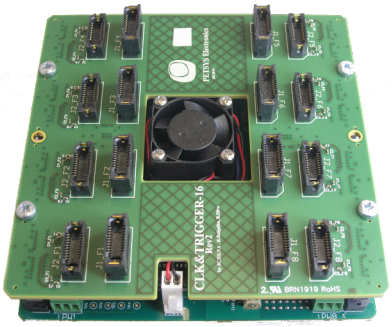

Figure 10: Clock&trigger unit.
Bottom view showing the connectors for 16 Samtec ERCD cables providing clock an trigger signals to the FEB/D units.

§ 4. The Clock&trigger unit.

All FEB/D units can be connected to the Clock&trigger (Fig. 10) unit using a flat coax cable Samtec ERCD-010-80.00-TBR-TBR-1-N. The Clock&trigger unit provides clock signals and synchronization signals to the FED/D unit, and allows implementing a system wide coincidence filter. It collects coarse time information from all the FEB/D units and tells the FEB/D units which events are part of a coincidence.

The Clock&trigger unit uses the same mother board as the FEB/D unit. It has the same communication mezzanine and uses the same communication protocol as the FEB/D units, and connects to the DAQ unit in the same way. It can be daisy-chained with the FEB/D units to connect to the DAQ unit.

The Clock&trigger unit supports up to 16 FEB/D units and 4 trigger regions per FEB/D.

For synchronization with external systems, Clock&trigger unit can accept an external clock and synchronization signal or it can provide a clock and synchronization signal to an external system. It can also accept a veto signal which causes all events across all FEM modules to be discarded when it's active.

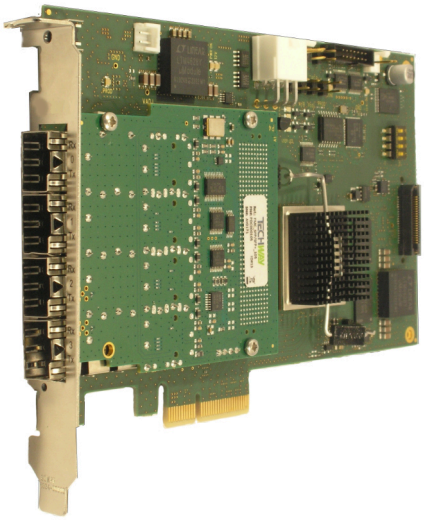

Figure 11: DAQ4 unit.
The DAQ4 unit plugs directly into the PCI express bus of the DAQ computer. The four SFP+ connectors on the front panel receive the four SFP+ copper links or optical links from the FEB/D chains.

§ 5. The DAQ unit.

The DAQ unit, the Clock&Trigger unit and the FEB/D units together form a complete and scalable data acquisition system that can handle tens of thousands of SiPM detector pixels.

The DAQ unit plugs in the DAQ computer and transmits the data to the DAQ computer using the PCI Express port. The DAQ unit receives data from the FEB/D units using a number of SFP+ optical or copper connectors connecting to chains of FEB/D units. Each chain of FEB/D units transmits data at 6.6 Gbps to the DAQ unit. This allows transmitting 100 M event records per second. The DAQ unit also distributes configuration files for the ASICs and configures the Clock&Trigger unit.

There are 2 versions of the DAQ unit: DAQ4 and DAQ16. The number refers to the number of SFP+ optical/copper connectors. The DAQ16 unit allows a much larger data rate to the computer. Until the middle 2024 we provided a version of the DAQ4 with only 3 SFP+ optical/copper connectors. Except for the number of SFP+ connectors the DAQ3 has the same characteristics as the DAQ4.

Main features of the DAQ4 unit.

- Single PCI Express board providing data acquisition with TOF ASICs.
- Equipped with Kintex 7 (xc7k325t) FPGA.
- Compatible with FEM128, FEM256, FEB/D-1k FEB/D-8k, and Clock&Trigger units.
- The DAQ4 has 4 PCI express Gen 2 lanes
- Equipped with 4 SFP+ optical/copper connectors receiving for optical links for sending and receiving data to and from four FEB/D unit chains.
- Maximum total input event rate: 100 M events/s for each of the input links.
- Maximum data output rate to the DAQ computer: 230 M events/s.
- Reads temperature sensors in the Front-End Modules.
- Reads internal counters in the TOFPET ASIC .
- Accepts an external veto signal and distributes it to the FEB/D boards via the Clock&Trigger unit.

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Main features of the DAQ16 unit.

- Single PCI Express board providing data acquisition with TOF ASICs.
- Equipped with Kintex Ultrascale+ (xcku11p) FPGA.
- Compatible with FEM128, FEM256, FEB/D-1k FEB/D-8k, andClock&Trigger.
- The DAQ16 has 16 PCI express Gen 3 lanes
- Equipped with 16 SFP+ optical/copper connectors sending and receiving data to and from FEB/D unit chains.
- Maximum total input event rate: 100 M events/s for each of the input links.
- Maximum data output rate to the DAQ computer: 1600 M events/s.
- Reads temperature sensors in the Front-End Modules.
- Reads internal counters in the TOFPET ASIC .
- Accepts an external veto signal and distributes it to the FEB/D unit via the Clock&Trigger unit.

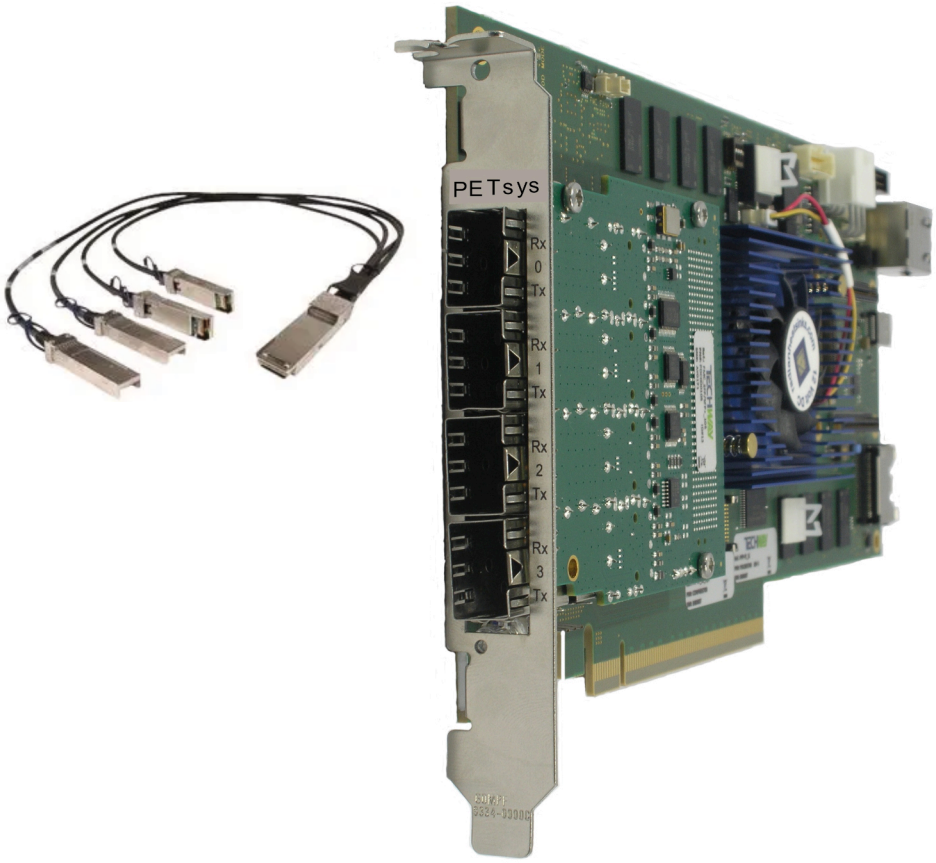

Figure 12: DAQ16 unit.
The DAQ16 unit plugs directly into the PCI express bus of the DAQ computer. The DAQ16 unit has 4 connectors on its front. Each takes one of the cable splitters shown on the figure to the left. This cable splitter provides 4 SFP+ connections that can take either a copper cable or an optical cable.

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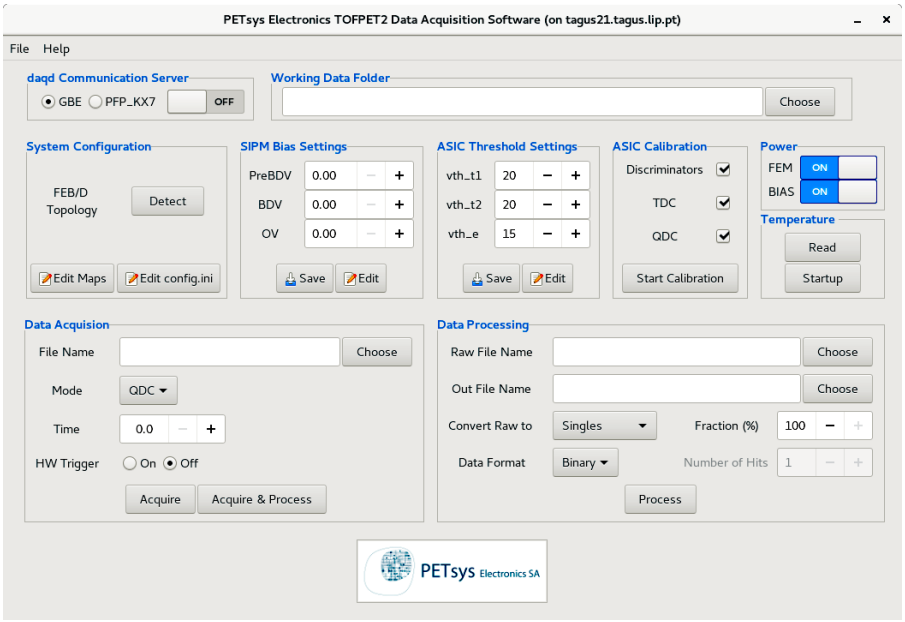

Fig. 13: Graphical user interface.
The data acquisition is controlled by an easy to use graphical user interface.

§ 6. Data acquisition firmware and software.

The PETsys readout system is provided with firmware and software. The data acquisition software runs under Linux (Red Hat Enterprise Linux 8.5 and above, CentOS 9 Stream, or Ubuntu 20.4 and above) and comes with an easy to use graphical user interface, see figure 13. The software is written in Python and C++, and is also provided as source code, allowing the advanced user to customize it under the MIT open source license.

The firmware implements a software centric approach, allowing direct and online access to PETsys TOFPET 2 ASIC configuration, to the bias voltage configuration, to the temperature sensor readout and to the uncalibrated (raw) TOFPET 2 ASIC data.

In order to reduce the data rate to the DAQ computer, the firmware in the FEB/D units supports coincidence event selection. The coincidence event selection is based on coarse time stamps (1 clock period, 5 ns). The complete readout system can be divided in a configurable number of trigger regions, and events without a coincidence partner in a different trigger region are discarded and not transmitted to the DAQ computer. The smallest trigger region consists of one quarter of one FEB/D unit, either FEB/D-1k or FEBD-8k. Besides the optional rejection of events that are not part of a coincidence, no other manipulation is performed on the raw event data from the TOFPET 2 ASIC.

The coincidence filter also allows to reject events based on the energy sum or multiplicity number (simultaneous events detected in the detector module. The time difference between coincidence events is configurable to 0, 1, 2 or 3 clock periods. When coincidences are found, the coincidence filter will forward any events within a window (3... 16 clock cycles) of the primary trigger events. The duration of the windows and the matching of the trigger regions is configurable.

The coincidence filter allows collecting of data for two types of random coincidence correction methods:

- Wide coincidence window: The coincidence window can be set to a value larger than2 clock cycles, allowing the collection of more random events; this is broadly equivalent to the delayed window method.
- Periodic single trigger: In addition to coincidences, the trigger can select all events in a window of 10, 20, 50 or100 clock periods every 1025 clock periods. The1025 clock periodicity ensures that the data collected is de-correlated from other reference clocks in the systems.

Synchronization with other systems.

It is often necessary to synchronize the clock on the PET readout with other clocks in the system. If the ratio of the clocks frequencies of the two sub systems is an integer, both can share a common clock and synchronization signal. The FEB/D unit or the Clock&trigger unit can accept an external signal and generate a event record with a time least count of 1.24 ns. Alternatively, one can use any ASIC input channel to generate time event records with a timing least count of 30 ps. Finally, the Clock&trigger unit can send out LVDS timing signals synchronized to the ASIC clock at a configurable frequency.

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§ 7. Examples of readout solutions.

The Front-End Modules, the Front End type D units, the DAQ unit and the Clock&Trigger unit together allow building data acquisition systems adapted to the needs of most applications. Below we present 3 typical applications.

Readout solution for small systems.

If the application requires 1'024 channels or less, and if the total data rate to the computer is below 15 M events/s after firmware coincidence event selection, the readout will need one FEB/D-1k unit equipped with an Ethernet communication mezzanine (Fig. 14). It can have a maximum eight FEM-128.

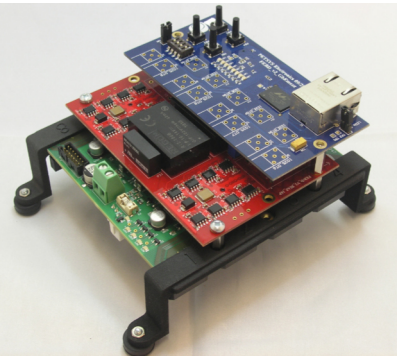


Figure 14. FEB/D-1k unit for small systems.

Figure showing a FEB/D-1k unit with Ethernet mezzanine. The FEB/D-1k unit collects data from up-to eight FEM128, and sends the data to a computer using an Ethernet link at 1Gbit/s.

Readout solution for several 1'000 channels.

If the application requires reading more than 1'024 channels, or requires a larger event rate to the computer, the system needs a Clock&Trigger unit and a DAQ unit.

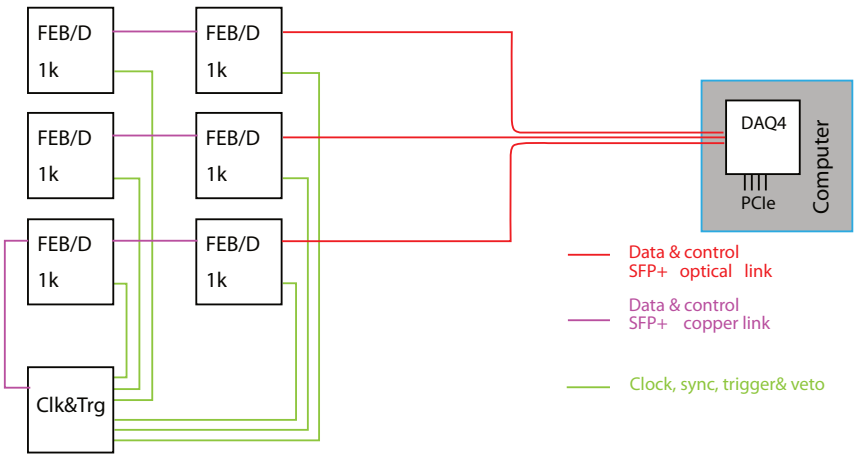
As an example, we show the system connection topology for a system with 6'144 channels in figure 15. Each FEB/D-1k unit is connected to eight FEM128. The communication between the master FEB/D-k unit and the DAQ4 computer uses optical fibers, and the communication between the FEB/D units in the FEB/D daisy chain uses SFP+ copper links. Each ASIC has 4 LVDS data output links, and the maximum data output rate from the ASIC to the FEB/D-1k is 500 kcps per ASIC channel.

In this example the data rate from the DAQ unit to the computer (230 M events/s) will be limiting the event rate per channel. Therefore, without the the firmware coincidence filter, the average maximum event rate per channel to the computer is limited to 38 kcps. The useful event rate will depend on the efficiency of the coincidence filter. The efficiency of the coincidence filter depends on the geometry of the PET scanner considered; it typically increases the effective average data rate per channel by a factor between 2 and 10.

If instead of the DAQ4 unit, a DAQ16 unit is used, each of the 6 FEB/D-1k can directly connect to the DAQ16 units using 2 SFP+ optical/copper links. In this case the average data rate per channel to the DAQ computer is limited by the connection between the FEB/D-1k to the DAQ unit, and the average data rate per channel to the DAQ computer can be up to to 200 kcps. Using the firmware coincidence filter will increase the useful rate until the limit of the ASIC is reached (500 kcps).

Figure 15. System with 6'144 channels.

System interconnect topology for a readout with 6 FEB/D-1k units.



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Readout solution for several 10’000 channels.

Applications such as Whole Body PET, require reading several 10’000 SiPM channels, and a lower cost per channel. Figure 16 shows the interconnect topology for a system reading 61’440 channels. It uses 240 FEM256 modules, 15 FEB/D-8k units, and two DAQ16 units. Each FEB/D-8k is connected to 16 FEM256. Each of the 15 FEB/D-8k directly connects to one of the DAQ16 units using 2 SFP+ optical/copper links. Therefore each FEB/D-8k can send 200 M event records per second to one of the DAQ16 units.

In the FEM256 module only 2 of the 4 data output lines per ASIC are used, and the maximum event rate from the ASIC to the FEB/D-8k is 300 kcps per channel. But the data rate will be limited by the connection between the FEB/D-8k and the DAQ16 unit. Without using the firmware coincidence selection, the average per channel data rate to the computer is limited to 50 k event records per second. The efficiency of the firmware coincidence filter depends on the detector module design and on the geometry of the PET scanner considered. The firmware coincidence filter typically increases the effective per channel data rate to the computer by a factor in the range 2 to 10.

The data rates mentioned above are only possible if DAQ computer is sufficiently powerful (multi-core high performance CPUs and SSDe NMVe disks).

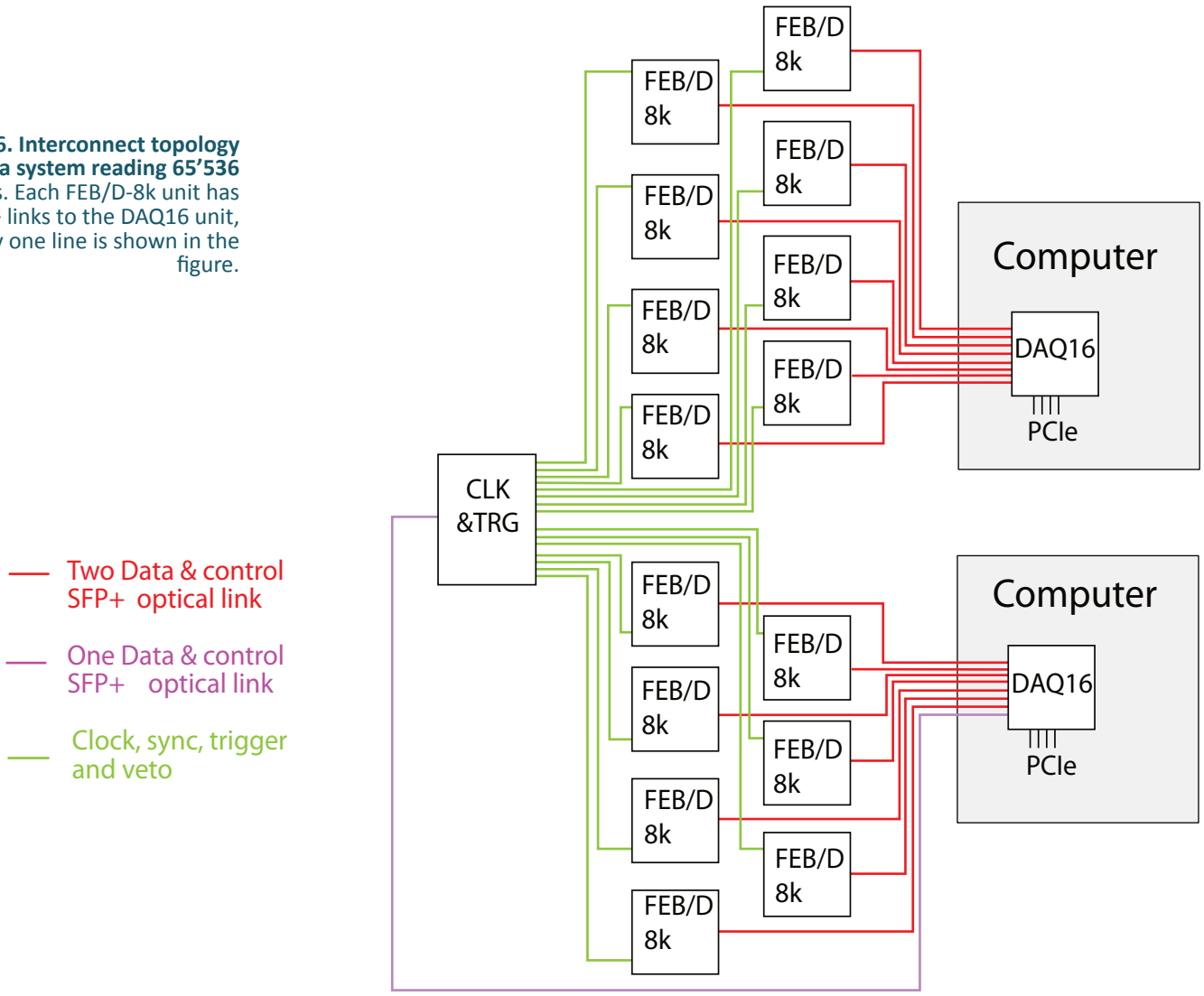

Figure 16. Interconnect topology for a system reading 65’536 channels. Each FEB/D-8k unit has two SFP+ links to the DAQ16 unit, but only one line is shown in the figure.

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Readout solution for reading more than 65’536 channels.

A total body PET scanner may require reading several 100’000 SiPM pixels. This will require either the development of a new FEM512 as front end board to read up to 512 SiPM pixel, or a new Clock&Trig unit supporting more than 16 FEB/D units.

Alternatively, one can reduce the number of electronic readout channels required by using some multiplexing scheme, although such schemes usually degrade the coincidence time resolution.

On our web site www.petsyselectronics.com/documentation there is extensive technical documentation about our electronics

Contact “sales@petsyselectronics.com” for any question

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