PETsys Electronics

TOFPET 2C/D
SiPM readout ASIC

General description

The TOFPET2 ASIC is a low-power, low-noise, readout and digitization ASIC implemented in 110nm CMOS technology for fast radiation detectors using Silicon Photomultipliers (SiPM) in Time-of-Flight (ToF) applications. The ASIC integrates signal amplification circuitry, discriminators, charge integration ADCs and high-performance TDCs for each of 64 independent channels. The pre-amplifier is a low impedance current conveyor. Two transimpedance post-amplifiers are optimized for time resolution and charge integration. Three voltage mode discriminators with configurable thresholds are used for timing measurements, to reject low amplitude pulses, to start the charge integration window, and to trigger the event data readout. Each channel has quad-buffered analogue interpolation TDCs with time binning of 30 ps and charge integration ADCs with linear response up to 1500 pC input charge. The ASIC requires 1.2 V and 2.5 V power supplies, two external voltage references and low-jitter LVDS clock.

Features

- Signal amplification and discrimination for each of 64 independent channels.
- Dual branch quad-buffered analogue interpolation TDCs for each channel.
- Quad-buffered charge integration for each channel.
- Dynamic range: 1500 pC.
- TDC time binning: 30 ps
- Gain adjustment per channel: 1, 1/2, 1/4, 1/8.
- SiPM family supported: positive input signal polarity
- Max channel hit rate: 500 kHz.
- Configurable timing, trigger and ToT thresholds.
- Fully digital output.
- Max output data rate: 3.2 Gb/s.

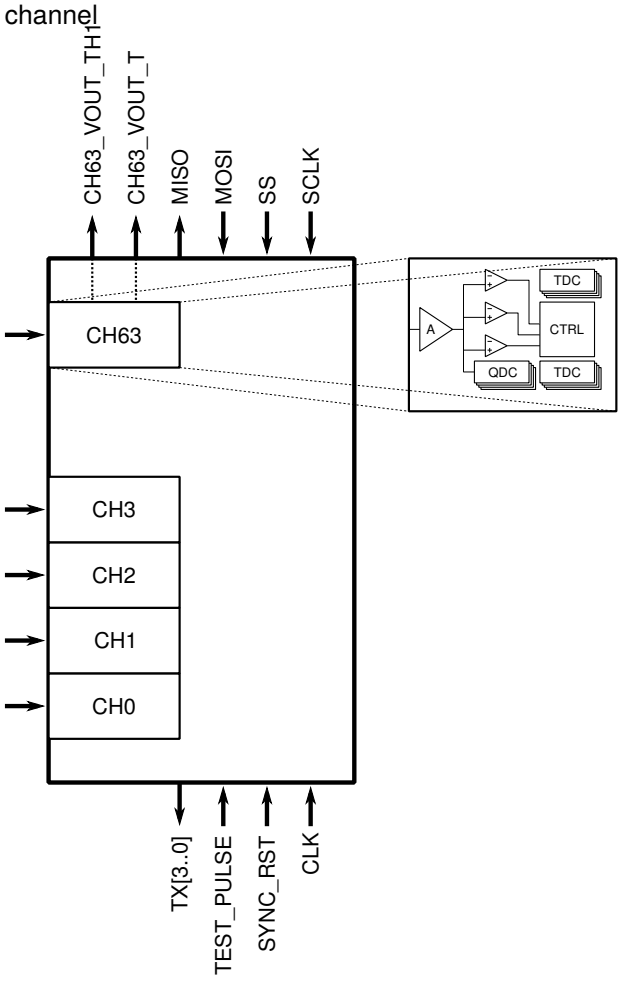
Applications

- Positron emission tomography.
- Cargo scanning.
- Nuclear and high energy physics experiments
- Radiation detection
- LIDAR

US patent no 7,917,192. Additional patents pending examination.

Functional block diagram

Figure 1: Functional block diagram of ASIC and channel



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Revision history

Revision number	Revision date	Description
18	2024/03/20	Corrected definition of bits 177 and 176 in table 12.
17	2023/09/05	Corrected maximum event output rate in table 2.
16	2022/09/20	Added errata to section 5.4.
15	2022/01/26	Correct miscelaneous typos in table 2, table 12 and missing reference to table 26.
14	2022/01/17	Clarification of global reset timing and sequence.
13	2021/07/12	Clarification and example code for CRC-8 calculation.
12	2021/04/13	Corrected settings in QDC mode.
11	2020/07/09	Added new section on trigger modes. Added new plots describing post-amplifier threshold and baseline behaviour. Added new information on VREF. Added settings for negative polarity input (TOFPET 2D only). Added settings for integration bias and it's effect on integration window length.
10	2019/09/24	Added missing option to table 19.
9	2019/05/24	Corrected QDC relative gains (section 5.7).
8	2019/04/29	Add description of data link heartbeat (section 7.4).
7	2019/01/21	Add note regarding delay line setting and trigger modes.
6	2018/11/23	Add plot of threshold DAC LSB settings.
5	2018/10/20	Discontinue support for negative input mode.
4	2018/08/30	Updated for TOFPET 2C. Users of TOFPET 2B should read the note on page 11.
3	2018/08/09	Corrected figure 40. Added subsection "11.3 Recommended footprint".
2	2018/07/06	Characterized TDC and QDC shift as function of temperature. Add description of expected signals on analog debug outputs. Add description of integration time window. Correction to figure 36. Correction to figures 18 and 19. Addition of figure 16. Add detail of resetting after configuration requirements in section 3. Add detail of resetting after configuration requirements in section 3. Correction of "integ_source_sw" bits in table 13. Correction of description of G_{Q1} and G_{Q2} settings in section 5.7.
1	2018/01/09	Initial release.

Table 1: Revision history

Contents

1 Specifications

Absolute maximum ratings

T_A = 24 °C unless otherwise noted.

- Functional operation of the device in Absolute Maximum Rating conditions or any conditions outside those specificed in Table 2 is not implied.
- Permanent exposure to Absolute Maximum Rating conditions can reduce device reliability.
- Exposure to conditions outside Absolute Maximum Rating conditions may cause permanent damage to device.

Table 2: Specifications

Description	Symbol	Min	Typ	Max	Units
Power supply					
1.2 V supply	$VDD12$	1.1	1.2	1.3	V
Total input current on $VDD12$ rails	I_{VDD12}		370	800	mA
2.5 V supply	VDD25	2.3	2.5	2.7	V
Total input current on VDD25 rails	I_{VDD25}		30		mA
External references					
Global voltage reference	VG	490	500	510	mV
Total input current on VG	I_{VG}			10	µA
TDC voltage reference	VREF	790	800	810	mV
Total input current on VREF	I_{VREF}	-0.2		10	mA
Analog inputs					
Input impedance	R_{IN}		20		Ω
Input DC voltage (positive input)	$V_{IN@P}$		800		mV
Input DC voltage (negative input)[a]	$V_{IN@N}$		400		mV
Input current	I_{IN}			20	mA
Input charge[g]	Q_{IN}			2300	pC
Transimpedance amplifier					
Transimpedance amplifier gain (T branch)	G_T		3000[b]		Ω
Transimpedance amplifier gain (E branch)	G_T		300[b]		Ω
Noise RMS (T branch)	V_{noise_T}		1.2[c]		mV
Saturation voltage of the TIA output stage	V_{sat}		400		mV
Time to Digital Converter (TDC)					
TDC binning	TDC_{LSB}		31[d]		ps
TDC resolution (RMS)	TDC_{RMS}		20[d]		ps
TDC DNL	TDC_{DNL}			0.1	LSB
TDC INL	TDC_{INL}			1.0	LSB
Charge to Digital Converter (QDC)					
Gain	G_Q	1.0	1.0	3.65	
QDC binning	QDC_{LSB}		3.6[e]		pC
Noise	QDC_{RMS}		0.7		LSB
QDC DNL	QDC_{DNL}			0.6[f]	LSB
QDC INL	QDC_{INL}			1.5[f]	LSB
QDC range			400		LSB
Integrator bias current	I_{integ_bias}		1.0		LSB/ns
Timing					
Main clock frequency	f_{CLK}	160		400	MHz
Event digitization clock frequency	f_{TDC_CLK}	160		200	MHz
SYNC_RST to CLK setup time[h]	t_{SU1}	1.0			ns
SYNC_RST to CLK hold time[h]	t_{H1}	0.25			ns
Configuration clock frequency	f_{SCLK}			10	MHz
Setup time to SCLK	t_{SU2}	20			ns
Hold time to SCLK	t_{H2}	20			ns
Output delay from SCLK	t_{CO2}	1		25	ns
Data transmission					
Output link rate		160		800	Mbit/s
Max event rate (per ASIC)				32	Mevent/s

[a] TOFPET 2D only.
[b] Adjustable down to ½, ¼, ⅛ of nominal.
[c] Measured with Hamamatsu S13361 SiPM at input.
[d] 200 MHz TDC_CLK.
[e] For $G_{Q1} \cdot G_{Q2} = 1.0$. Adjusting the gain trades dynamic range for resolution.
[f] Over a range of 160 LSB.
[g] Dependent on pulse shape. Indicative value for pulses generated by KETEK-PM3325-WB SiPM with 40 ns decay time coupled to LYSO scintillating crystal.
[h] Setup and hold time from SYNC_RST to SCLK are t_{SU2} and t_{H2}.

Table 3: Absolute maximum ratings

Description	**Rating**
ESD	2kV
VDD12 to GND	-0.2 to 1.4V
Analog input to GND	-0.2 to 1.4V
VDD25 to GND	-0.2 to 2.8V
Digital input to GND	-0.2 to 2.8V
Digital outptu to GND	-0.2 to 2.8V
Junction Temperature	125 °C

2 Power and biasing

Figure 2: Power and biasing

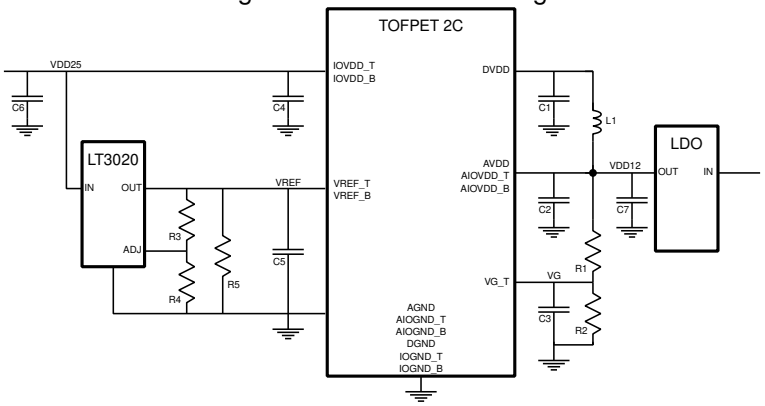


Figure 2 shows the recommended scheme for supplying power and bias to TOFPET 2C.

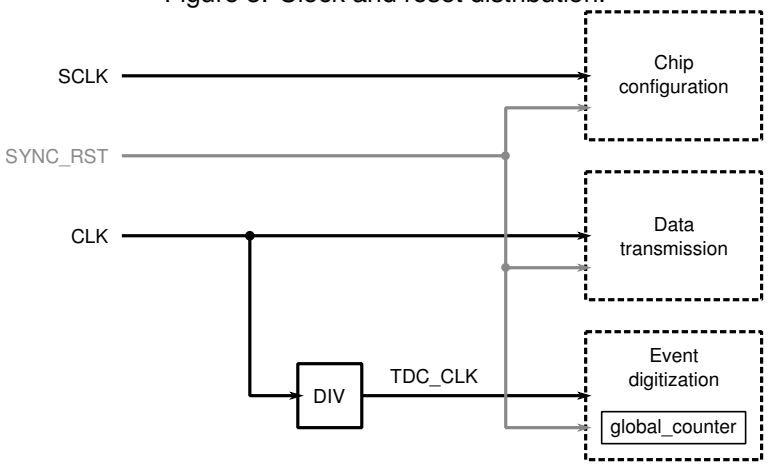
- *VDD*12 should be provided by a linar regulator close to the device. Any noise in the *VDD*12 supply rail will contribute to degrading device performance.
- Variations in *VDD*12, *VG* and *VREF* even within the operation range will change the devices operation characteristics and require re-calibration.
- A LT3020 LDO and respective R3 and R4 adjustment resistors is shown as means to generate VREF. The values used for R3 and R4 are necessarily low because the VREF pins can also source current. Other similar LDO models can be used to generate VREF but the same care must be taken to use low values for the adjustment resistors.
- A resistive divider (R1 and R2) is shown as means to generate VG. A 500 mV voltage reference is also suitable.
- Load resistor R5 is used to ensure the minimum current drawn from the LDO is within it's specifications. In particular the designer should beware that the TOFPET 2's VREF pin can draw or source current.

Table 4: Reference values

Symbol	Values	Description
R1	1100 Ω	
R2	787 Ω	
R3	330 Ω	
R4	110 Ω	
R5	660 Ω	
L1	100 Ω @ 100 MHz	Ferrite bead.
C1	100 nF, 10 nF	Decoupling capacitance. Place multiple close to TOFPET 2C.
C2	100 nF	Decoupling capacitance. Place multiple close to TOFPET 2C.
C3	1 µF, 100 nF	
C4	100 nF	
C5	1 µF, 100 nF	Decoupling capacitance. Place multiple close to TOFPET 2C.
C6	100 nF	Bulk capacitance.
C7	100 nF	Bulk capacitance.

3 Clocking and resetting

Figure 3: Clock and reset distribution.



TOFPET 2C has two independent (asynchronous) clock domains.

- SCLK which drives the ASIC configuration logic. This clock can be gated off during the normal ASIC operation.
- Core clock (CLK) which drives all the core logic (event digitization and transmission).
  - Data transmission links are driven directly by CLK.
  - Event digitization is driven by CLK divided by a factor DIV, set by global setting tdc_clk_div. This includes the *global_counter* coarse counter which is the basis for the coarse event time tags.

Table 5: DIV setting

tdc_clk_div	DIV value
0b0	1
0b1	2

Reset

The two clock domains share a single reset signal SYNC_RST.

- If SYNC_RST is active during a CLK rising edge, the logic driven by CLK will be reset.
- If SYNC_RST is active during a SCLK rising edge, the logic driven by SCLK, including the ASIC configuration registers, will be reset.

In some circumstances, the general, the core logic MUST be reset after a channel configuration write or read.

- The core logic MUST be reset after changing the contents of global channel register for which CRR is “YES” (see table 12).
- The core logic MUST be reset after ANY channel configuration write or read.

A typical sequence for “TOFPET 2C” operation is

1. Power on.
2. Enable CLK.
3. Reset all logic:
   - Enable SYNC_RST.

- Enable SCLK.
- Disable SCLK.
- Disable SYNC_RST.

4. For each configuration register:
    - Enable SCLK.
    - Write configuration register.
    - Disable SCLK.
5. Pulse SYNC_RST to reset core logic.

4 Configuration interface

The ASIC configuration consists of a 184-bit global configuration vector and a 125-bit per channel configuration vector, which can be written or read through the configuration interface. The configuration interface is a 4-signal interface similar to SPI but implemented using LVDS signalling. Also of note, MISO does not have tri-state capability.

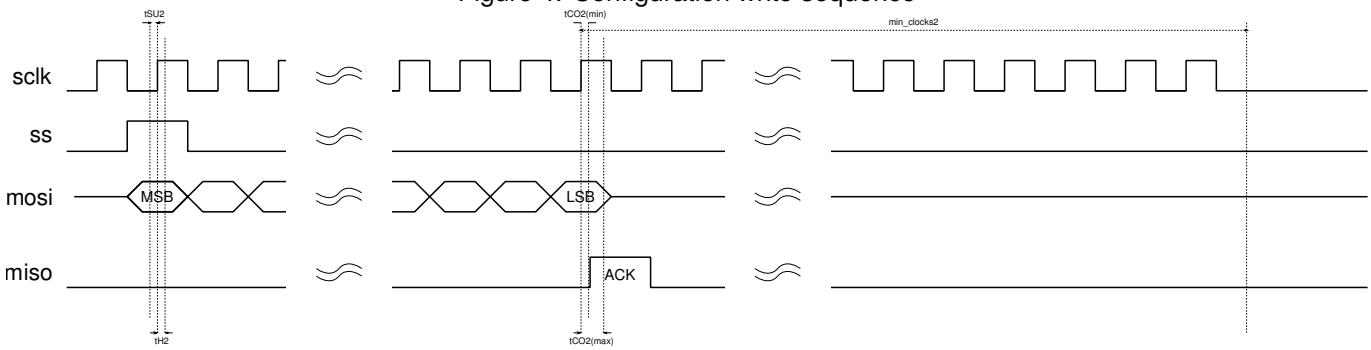
The configuration commands and replies are protected by an 8-bit CRC, whose polynomial is $x^8 + x^2 + x + 1$ and initial value is 0x8A. See section A for example code.

Figure 4 and table 2 lists the timing requirements for the configuration interface. The configuration clock SCLK can be disabled when not needed, but it should be kept active for a minimum of 200 clock (*min_clocks2*) after an acknowledgement in order for the internal configuration state machine to settle.

4.1 Write

To write a configuration vector, the SPI master asserts SS for 1 clock cycle and transmits the configuration command on MOSI. If the command is successfully received, the ASIC will acknowledge it by asserting the MISO signal for one clock period.

Figure 4: Configuration write sequence



4.1.1 Global configuration write command

The global configuration write command is a 196-bit vector, transmitted MSB first, as per table 6.

4.1.2 Channel configuration write command

The channel configuration write command is a 144-bit vector, transmitted MSB first, as per table 7.

Table 6: Global configuration write command

Bits	Content
195:192	0b1000
191:8	Configuration register content (184-bit).
7:0	8-bit CRC of the preceding bits.

Table 7: Channel configuration write command

Bits	Content
143:139	0b00000
138:133	Channel number.
132:8	Configuration register content (125-bit).
7:0	8-bit CRC of the preceding bits.

4.2 Read

To read a configuration vector, the SPI master asserts SS for 1 clock cycle and transmits the configuration command on MOSI. If the command is successfully received, the ASIC will acknowledge it by asserting the MISO signal for one clock period and then will transmit the reply on the MISO signal.

4.2.1 Global configuration read command

The global configuration read command is a 12-bit vector, transmitted MSB first, as per table 8. If successfully acknowledged, the ASIC replies with a 192-bit vector as per table 9.

Figure 5: Configuration read sequence

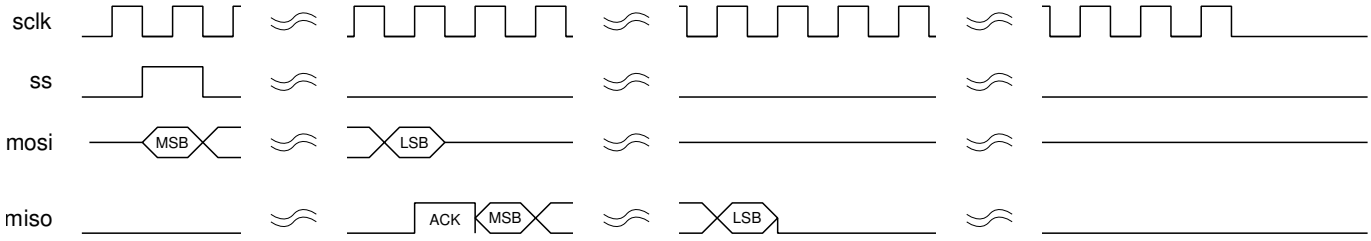


Table 8: Global configuration read command

Bits	Content
11:8	0b1001
7:0	8-bit CRC of the preceding bits.

Table 9: Global configuration read reply

Bits	Content
191:8	Configuration register content (184-bit).
7:0	8-bit CRC of the preceding bits.

4.2.2 Channel configuration read command

The channel configuration read command is a 19-bit vector, transmitted MSB first, as per table 10. If successfully acknowledged, the ASIC replies with a 133-bit vector as per table 11.

Table 10: Channel configuration read command

Bits	Content
18:4	0b00010
13:8	Channel number.
7:0	8-bit CRC of the preceding bits.

Table 11: Channel configuration read reply

Bits	Content
132:8	Configuration register content (125-bit).
7:0	8-bit CRC of the preceding bits.

4.3 Configuration register fields

The following tables contain the description of the configuration register fields as well as default values to be set in TOFPET 2C configuration registers.

- The values here are *not* the values present in the configuration registers after a reset (see 3).
- For fields without description, PETsys does not at this time support modifying their values.
- Note some fields use big endian bitness, while other fields use little endian bitness.

Note for TOFPET 2B users

TOFPET 2C is backward compatible with TOFPET 2B regarding package and performance, but there are some differences between the contents of the configuration registers for TOFPET 2B and TOFPET 2C.

- Global config *fe_ib*2 has 6 instead of 5 bit and a different default value.
- Global config *main_global_dac* has a different default value.
- Global config *counter_period* has a different format and different default value. See section 5.9.
- Channel configs *min_intg_time* and *max_intg_time* have a different format and different default value. See section 5.7.
- Channel config *ch*63*_obuf_msb* has been replaced with global configuration *adebug_buffer*. See section 6.1.

4.3.1 Global configuration register

Description	Bits	Default value	Symbol	Section	DD1R
Set number of active links	1...0	0b10	tx_nlinks	7	YES
Set link rate mode (SDR or DDR)	2...2	0b1	tx_ddr	7	YES
Set link mode	4...3	0b10	tx_mode	7.1	NO
Enable digital debug output mode	5...5	0b0	debug_mode	6.2	YES
Enable Trigger veto.	11...6	0b000000	veto_mode	5.4	YES
Set TDC clock divider	12...12	0b1	tdc_clk_div	3	YES
	15...13	0b110	r_clk_en		YES
	17...16	0b00	n/u		
	19...18	0b00	stop_ramp_en		YES
Set event counter enable	20...20	0b0	counter_en	5.9	YES
Set event counter period	23...21	0b110	counter_period	5.9	YES
	24...24	0b1	tac_refresh_en		YES
	28...25	0b1001	tac_refresh_period		YES
	30...29	0b00	data_clk_div		YES
	31...31	0b0	n/u		
	32...32	0b0	fetp_enable		NO
Set input polarity	33...33	0b1	input_polarity	5.1	NO
	34...39	0b101111	attenuator_ls		NO
	40...45	0b111001	v_ref_diff_bias_ig		NO
	46...50	0b11111	v_cal_ref_ig		NO
	51...55	0b10111	fe_postamp_t		NO
	56...60	0b10100	fe_postamp_e		NO
	61...65	0b00001	v_cal_tp_top		NO
	66...70	0b00000	v_cal_diff_bias_ig		NO
	71...76	0b100011	v_att_diff_bias_ig		NO
	77...82	0b111011	v_integ_ref_ig		NO
	83...87	0b10111	imirror_bias_top		NO
	88...92	0b00100	tdc_comp_bias		NO
	93...97	0b10011	tdc_i_lsb		NO
Set LSB of T1 threshold DAC	98...103	0b111010	disc_lsb_t1	5.2	NO
	176, 104...108	0b110000	fe_ib2		NO
	109...114	0b110110	vdifffoldcas		NO
	115...118	0b1110	disc_vcas		NO
Set LSB of E threshold DAC	119...124	0b101000	disc_lsb_e	5.3	NO
	125...129	0b10010	tdc_i_ref		NO
	130...133	0b0010	tdc_comp_vcas		NO
	134	0b1	fe_ib2_x2		NO
	135...139	0b10111	main_global_dac		NO
	140...145	0b111011	fe_ib1		NO
	146...151	0b010011	disc_ib		NO
Set LSB of T2 threshold DAC	152...157	0b110000	disc_lsb_t2	5.2	NO
	158...162	0b01101	tdc_tac_vcas_p		NO
	163...166	0b0111	tdc_tac_vcas_n		
Enable channel 63 analog debug outputs	167...168	0b11	adebug_out_mode	6.1	NO
	169...174	0b010011	tdc_global_dac		NO
Analog debug outputs buffer strength	175	0b1	adebug_buffer	6.1	NO
	177	0b0	n/u		
	178...183	0b100000	disc_sf_bias		NO

Table 12: Global configuration register content

4.3.2 Channel configuration register

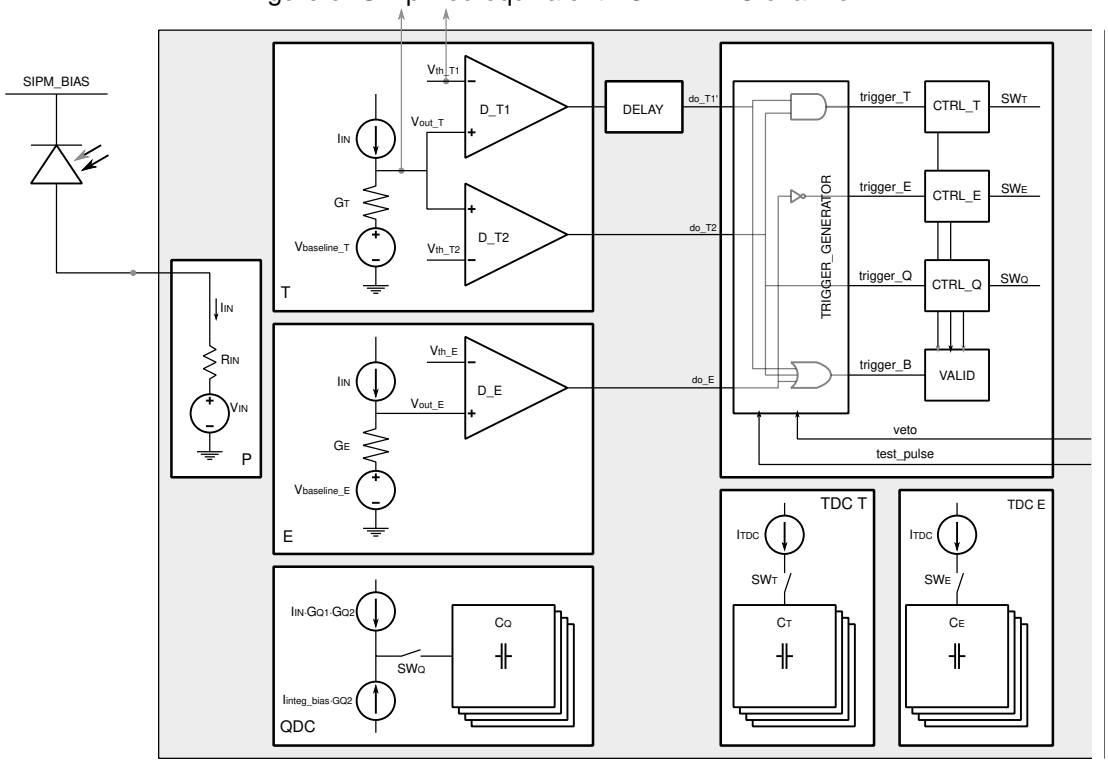
Description	Bits	Default value	Symbol	Section
Set trigger mode	1...0	0b00	Set trigger_mode_1	5.4
Enable digital debug output mode	3...2	0b00	debug_mode	6.2
	5...4	0b00	sync_chain_length	
Set additional channel dead time	11...6	0b000000	dead_time	5.8
Set event counter mode	15...12	0b0000	counter_mode	5.9
	20...16	0b11110	tac_max_age	
	25...21	0b01010	tac_min_age	
Set trigger mode	27...26	0b01	Set trigger_mode_2_t	5.4
Set trigger mode	30...28	0b010	Set trigger_mode_2_e	5.4
Set trigger mode	32...31	0b01	Set trigger_mode_2_q	5.4
Set trigger mode	35...33	0b101	Set trigger_mode_2_b	5.4
	36...36	0b1	branch_en_eq	
	37...37	0b1	branch_en_t	
Set ToT or QDC mode	38...38	0b1	qdc_mode	5.5
	39...39	0b0	Set trigger_b_latched	
Set QDC minimum integration time	46...40	0b0100010	min_intg_time	5.7
Set QDC maximum integration time	53...47	0b0100010	max_intg_time	5.7
Set input polarity	55...54	0b00	output_en	5.1
	56...56	0b0	qtx2_en	
Set post-amplifier T baseline	62...57	0b111101	baseline_t	5.2
Set T1 discriminator threshold	68...63	0b111000	vth_t1	5.2
Set T2 discriminator threshold	74...69	0b101111	vth_t2	5.2
Set E discriminator threshold	80...75	0b010011	vth_e	5.3
Set post-amplifier E baseline	82, 83, 81	0b110	baseline_e	5.3
do_T1 delay	84, 88, 87, 85, 86	0b01110	fe_delay	5.4
Set post-amplifier T gain	89...90	0b00	postamp_gain_t	5.2
Set post-amplifier E gain	91...92	0b00	postamp_gain_e	5.3
	94...93	0b00	postamp_sh_e	
Enable QDC mode	95...95	0b1	intg_en	5.5
Enable QDC mode	96...96	0b1	intg_signal_en	5.5
Set integrator gain	99...97	0b001	att	5.7
	103...100	0b0000	tdc_current_t	
	107...104	0b0000	tdc_current_e	
	109...108	0b00	fe_tp_en	
	110	0b1	n/u	
Set integrator gain	112...111	0b00	integ_source_sw	5.7
	117...115	0b010	t1_hysteresis	
	120...118	0b010	t2_hysteresis	
	123...121	0b010	e_hysteresis	
	124...124	0b1	hysteresis_en_n	

Table 13: Channel configuration register content

5 Channel

TOFPET 2C consists of 64 independent channels, each containing independent amplifiers, discriminators, time-to-digital converters and charge-to-digital converters (figure 6).

Figure 6: Simplified equivalent TOFPET 2C channel.



- The input stage (P) provides a low impedance input (R_{IN}) to the sensor's output current signal.
- The input current I_{IN} is then replicated into 3 branches: T, E and Q.
- T and E branches feed into discriminators which are used to control the trigger logic.
- Q branch integrates a replica of the input current, which can then be digitized by an internal ADC.

5.1 Input stage

- With TOFPET 2D the input stage can be configured to accept positive or negative input pulses as per table 14
- The input has a DC offset for internal biasing, which depends on the polarity selection.

Table 14: Input polarity selection

input_polarity	output_en	Input polarity	V_{IN}	
0b1	0b00	Positive	800 mV	
0b0	0b01	Negative	400 mV	Only with TOFPET 2D.

5.1.1 Input stage impedance tuning

The input stage has an adjustable bias current I_{B1} (see figure 7) which sets the input impedance R_{IN} as per figure 8.

- Any significant current sourced or sunk by the TOFPET 2C from the sensor will add to I_{B1} and thus shift the operation point.

Figure 7: Input stage bias I_{B1} versus fe_ib1

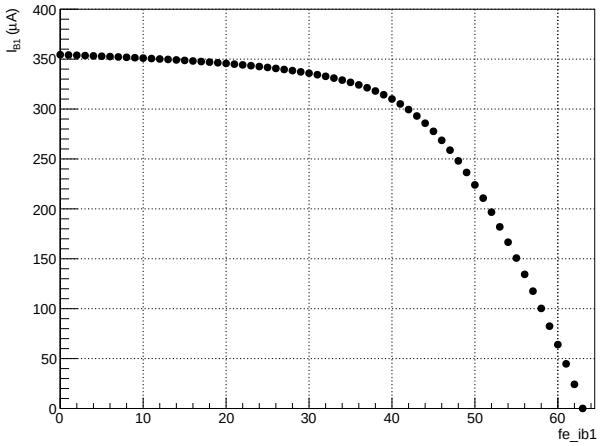
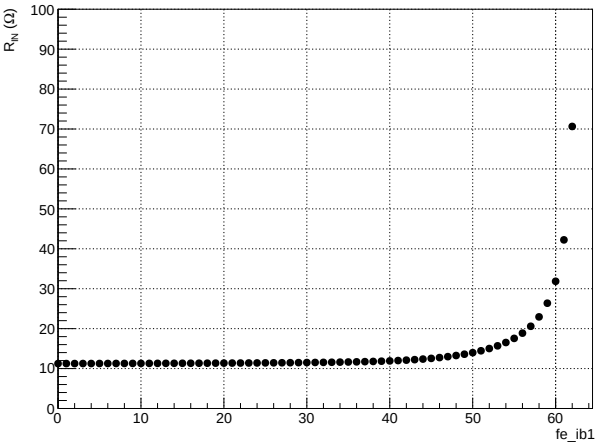


Figure 8: Input stage impedance versus fe_ib1



5.1.2 Performance versus power consumption

The input noise V_{noise_T} is a function of the capacitance at the input and of the setting fe_ib2 and fe_ib2_x2, but these settings also have a major effect in TOFPET 2C power consumption (figure 22).

The default value setting has been experimentally verified by PETsys as resulting in the good timing measurement when reading positively biased SiPM with a good power consumption. However, on a per application basis, different trade-offs can be made between power and noise.

5.2 Transimpedance amplifier (branch T)

Table 15: Transimpedance gain (T)

postamp_gain_t	G_T
0b00	3000 Ω (nominal)
0b10	1500 Ω
0b01	750 Ω
0b11	375 Ω

Table 16: Transimpedance gain (E)

postamp_gain_e	G_E
0b00	300 Ω (nominal)
0b10	150 Ω
0b01	75 Ω
0b11	38 Ω

The transimpedance amplifier converts the replica of the input current I_{IN} into a voltage V_{out_T} with gain G_T plus an offset $V_{baseline\_T}$. G_T is adjustable (see table 15). The amplifier saturates for $V_{out\_T} > V_{sat}$.

V_{out_T} connects to two identical discriminators (D_T1 and D_T2) whose threshold voltages (V_{th_T1} and V_{th_T2}) are set by 6-bit DACs vth_t1 and vth_t2 respectively. The offset $V_{baseline\_T}$ is set by another 6-bit DAC baseline_t and is used to trim the the baseline of V_{out_T} relatively to the input of the discriminators.

Important notes:

- vth_t1 and vth_t2 should not be set to 0b111111.
- baseline_t should not be set to 0b111111.
- The setting of $V_{baseline\_T}$, V_{th_T1} and V_{th_T2} are affected by the global settings disc_lsb_t1 and disc_lsb_t2 respectively, according to figure 9 and 10.
- V_{out_T}, V_{th_T1} and V_{th_T2} approach saturation at ≈900 mV.

Figure 9: V_{th_T1}

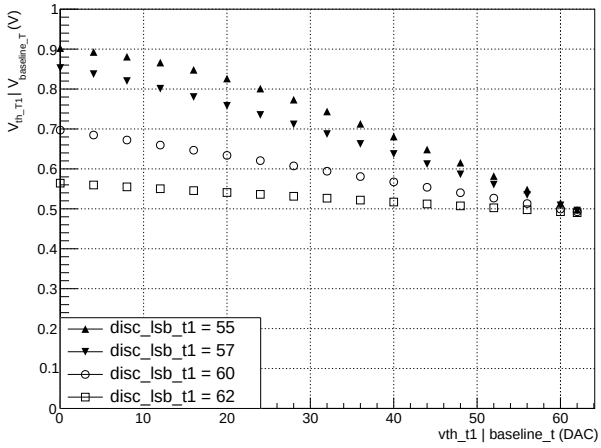
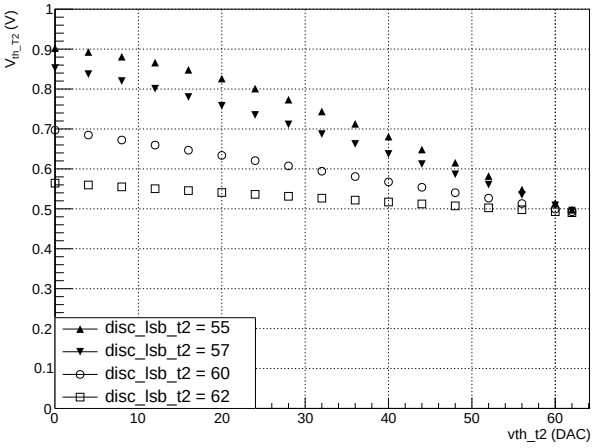


Figure 10: V_{th_T2}



5.3 Transimpedance amplifier (branch E)

Branch E is similar to branch T, with the following differences:

- Gain G_E is lower (see table 16), allowing a higher range of signals before saturation.
- It feeds a single discriminator D_E.
- $V_{baseline\_E}$ is set by a 3-bit DAC.

Important notes:

- vth_e should not be set to 0b111111.
- baseline_e should not be set to 0b111.
- V_{th_E} is affected by the global setting disc_lsb_e, according to figure 11.
- Both V_{out_E} and V_{th_E} approach saturation at ≈900 mV.

Figure 11: V_{th_E}

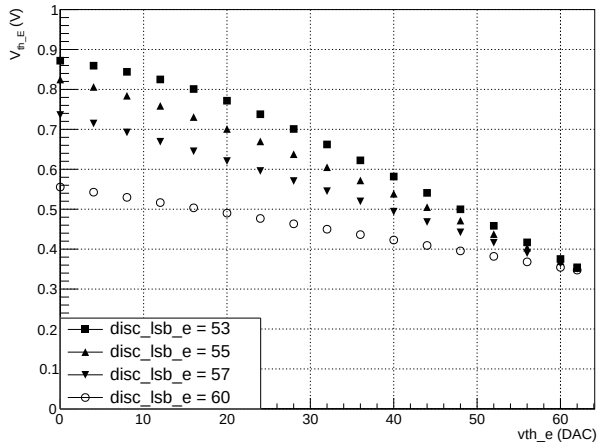
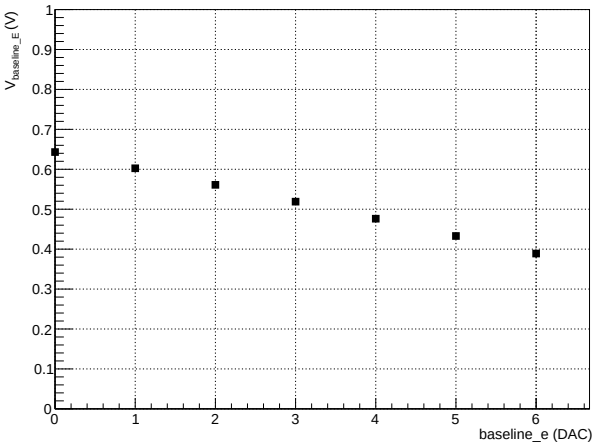


Figure 12: $V_{baseline\_E}$



5.3.1 Performance versus power consumption

The slew rate of the discriminators V_{noise_T} is a function of the capacitance at the input and of the setting *sf_disc_bias*, but this settings also has an effect in TOFPET 2C power consumption (figure 23).

The default value setting has been experimentally verified by PETsys as resulting in the good timing measurement when reading positively biased SiPM with a good power consumption. However, on a per application basis, different tradeoffs can be made between power and noise.

5.4 Event trigger logic

The output of the 3 discriminator connects to TRIGGER_GENERATOR logic box which generates 4 trigger signals: trigger_T, trigger_Q, trigger_E and trigger_B, according to the logic expressions in tables 18 to 22.

- The output of discriminator T1 (do_T1) passes through a configurable delay line (do_T1'), as per table 17.
- The discriminators can be replaced by test_pulse, as per table 18.

The trigger processing is illustrated by figure 13.

1. The trigger logic starts in the READY state, prepared to accept an upcoming event.
2. The state moves from READY to TRIGGERED state upon a rising edge of either trigger_T, trigger_E or trigger_Q.
3. The state moves from TRIGGERED to event VALIDATE when trigger_B is zero.

   An event is valid if rising edges have been detected on all of trigger_T, trigger_E and trigger_Q. In this case, the logic moves to ACCEPT, queueing the event for digitization and transmission.

   If only one or two of trigger_T, trigger_E and trigger_Q had rising edges, the logic moves to DISCARD, queueing the event for rejection.
4. After ACCEPT or DISCARD, the logic moves to REARM and then to READY again.

Figure 13: Trigger processing states.

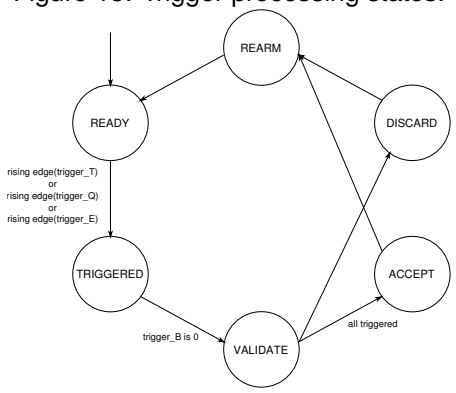


Table 17: D_T1 delay settings

fe_delay	Delay line length
0b01101	3 ns
0b01110	6 ns
0b01111	8 ns
0b10000	OFF (Delay line bypassed)

Table 18: Channel trigger mode

trigger_mode_1	Description
0b00	Normal trigger using discriminators' output.
0b01	All discriminators are replaced by test_pulse.
0b10	All discriminators are inverted.
0b11	Channel disabled.

Table 19: trigger_T generation

trigger_mode_2_t	trigger_T
0b00	$do\_T1' \dagger$
0b01	$do\_T1' \cdot do\_T2 \ddagger_{(nominal)}$
0b10	$do\_T1' \cdot do\_E \ddagger$
0b11	do_E

Table 20: trigger_Q generation

trigger_mode_2_q	trigger_Q
0b00	do_T1'
0b01	do_T2 (nominal)
0b10	do_E

- †This trigger mode should only be used with delay line set to OFF.
- ‡This trigger mode should not be used with delay line set to OFF.

For more information see section 9.

Table 21: trigger_E generation

trigger_mode_2_e	trigger_e
0b000	$\overline{do\_T1'}$
0b001	$\overline{do\_T2}$
0b010	$\overline{do\_E}$ (nominal)
0b011	$\overline{do\_T1' \cdot do\_T2}$ ‡
0b100	$\overline{do\_T1' \cdot do\_E}$ ‡
0b101	do_T1'
0b110	do_T2
0b111	do_E

Table 22: trigger_B generation

trigger_mode_2_b	trigger_B
0b000	do_T1'
0b001	do_T2
0b010	do_E
0b011	$do\_T1' + do\_T2$
0b100	$do\_T1' + do\_E$
0b101	$do\_T1' + do\_T2 + do\_E$ (nominal)

Table 23: Veto setting

veto_mode	Trigger mode.
0b000000	Normal operation.
0b000001	Triggering is inhibited for all channels when input SS is active.
0b000010	Triggering is inhibited for all channels when input TEST_PULSE is active.
0b000011	Triggering is inhibited for all channels when either input SS or TEST_PULSE is active.

Errata

- When `trigger_mode_1` is set to `0b01` there is a ≈400 ps window in each clock cycle where TOFPET 2 fails to detect the triggers. This behaviour is not observed in normal operation.
- In normal operation with high dark event rates a fraction of detected events have their timestamps offset by $\approx \pm 300$ ps. No work around is known for these except to reduce dark event rate (e.g. by lowering sensor bias voltage).

5.5 Measurement mode

Table 24: TOFPET channel measurement modes

qdc_mode	intg_en	intg_signal_en	Measurement mode
0b1	0b1	0b1	Time and charge (QDC) mode.
0b0	0b0	0b0	Dual time (ToT) mode.

Time and Charge (QDC) mode

In this mode the ASIC performs

- The TDC T measures the time of the rising edge of trigger_T.
- The QDC measures the integrated charge from the rising edge of trigger_Q until the end of the integration window (section 5.7).
- Valid even require rising edges on trigger_T, trigger_Q and trigger_E.
- trigger_E is used only for energy selection and the TDC E is unused.

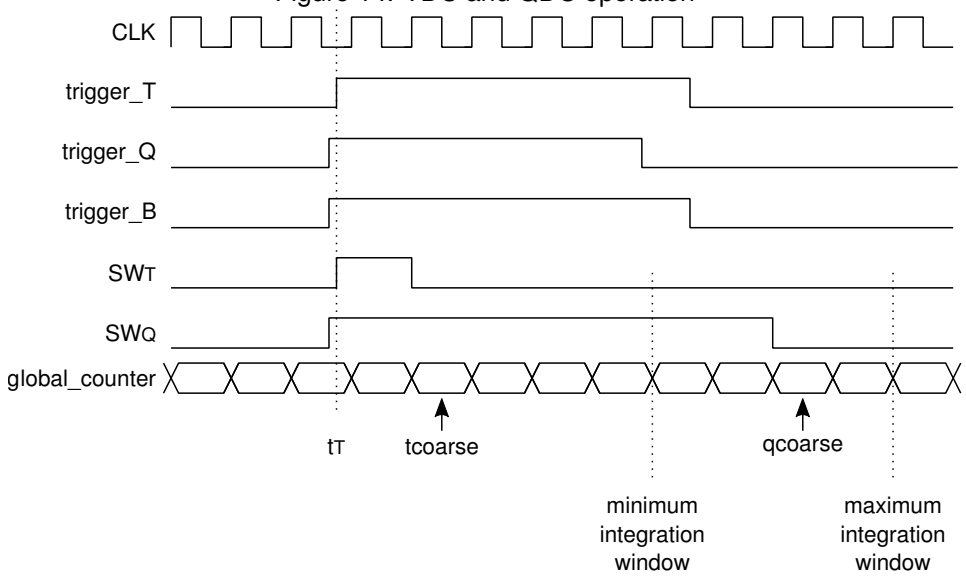
Dual time (ToT) mode

In this mode the ASIC performs

- The TDC T measures the time of the rising edge of trigger_T.
- The TDC E measures the time of the rising edge of trigger_E.
- Valid even require rising edges on trigger_T and trigger_E.
- trigger_Q is ignored and QDC is unused.

5.6 TDC

Figure 14: TDC and QDC operation



TDC operation is illustrated in figure 14.

1. On the rising edge of trigger_T switch SW_T closes, charging analog buffer C_T with current I_{TDC}.
2. On the 2nd next rising edge of CLK, SW_T opens, stopping the charging process.
3. The value of a global_counter is latched on the next clock providing value *tcoarse*.

If the event is valid, the voltage stored in C_T will be digitized as *tfine*.
In first approximation, the time t_T of the rising edge of trigger_T can be calculated as per equation 1.

$$t_T = tcoarse - \frac{tfine}{I_{TDC}} \tag{1}$$

where $I_{TDC} = \frac{1}{TDC_{LSB}}$.
The E TDC operates identically, using trigger_E signal and producing *ecoarse* and *efine* values.

5.7 QDC

QDC operation is illustrated in figure 14.

1. On the rising edge of trigger_Q switch SW_Q closes, charging analog buffer C_Q with a replica of the input current signal $I_{IN} \cdot G_Q$ plus a DC current I_{integ_bias}.
2. SW_Q opens on a rising edge of CLK when either
   - trigger_B is zero and minimum integration time (*min_intg_time*) has been met.
   - Maximum integration time (*max_intg_time*)has been reached.
3. The value of a global_counter is latched on the next clock providing value *qcoarse*.

Thus, the total charge stored in C_Q is given by equation 2.

$$Q_{total} = \int_{rise(SW_Q)}^{fall(SW_Q)} \left(I_{IN} \cdot G_Q + I_{integ\_bias}\right) \tag{2}$$

If the event is valid, the charge stored in C_Q, minus an offset Q_{offset} will be digitized as *qfine*.

$$qfine = Q_{total} - Q_{offset} \tag{3}$$

The time of $fall\,(SW_Q)$ is given by *qcoarse* while the time of $rise\,(SW_Q)$ can be approximated by t_T. Thus, in first approximation, the input signal charge Q_{IN} can be calculated as per equation 4.

$$Q_{IN} = \int_{rise(SW_Q)}^{fall(SW_Q)} I_{IN} = \frac{qfine - I_{integ\_bias} \cdot (qcoarse - t_T) - Q_{offset}}{G_Q} \tag{4}$$

Integrator gain and range

The gain of the integrator (G_Q) is configurable.

- G_Q affects the dynamic range of the input current (table 25).
- G_Q also affects offset and gain relative to I_{integ_bias}. Different G_Q settings require different ASIC calibrations.

Table 25: Integrator gain G_{Q1}

att	v_att_diff_bias_ig	G_{Q1}
0b000	0b100011	2.5
0b001	0b100011	1.00
0b011	0b111000	1.70
0b100	0b100011	3.65
0b101	0b100011	1.39

Integration time

The integration time can be set either as a window (*min_intg_time* < *max_intg_time*) or as a fixed value (*min_intg_time* = *max_intg_time*). The settings are as per table 27.

The range of usable integration window lengths depends on the value of I_{integ_bias} as shown in figure 15. I_{integ_bias} can be adjusted as per table 26.

Figure 15: qfine as function of integration window length.

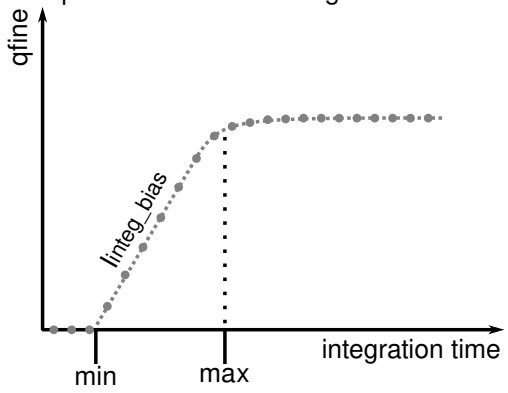


Table 26: Integrator bias I_{integ_bias}

imirror_bias_top	Typical usable integration window (ns)
23	250 – 500
26	375 – 750
29	875 – 1625
30	1500 – 2100

Table 27: Integrator window settings

Configuration value (N)	Actual integration time (TDC_CLK periods)	
	TOFPET 2C	TOFPET 2B
0...15	N	
16..31	$2 \times N - 16$	$4 \times N$
32..127	$4 \times N - 78$	

5.8 Multi-buffering

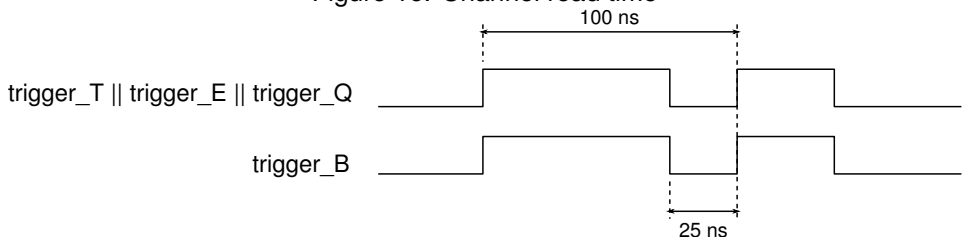
Each channel has 4 sets of C_T, C_E and C_Q analog buffers (figure 6) where analog values are stored before being digitized. Every time the channel goes through REARM state (figure 13), a new buffer set is selected round-robin. This allows the channel to rearm without waiting for the previous event to be digiti. When an event is valid and digitized, the *tac_id* number of the analog buffer set used to process that event is transmitted along the event.

Due to process variations, each analog buffer should be calibrated for optimal results.

Dead time

- Minimum dead time between TRIGGERED and READY is 100 ns.[1]
- Minimum dead time between VALIDATE and READY is 25 ns.[1]
- Maximum rearm rate is 10 MHz.[1]

Figure 16: Channel read time



Additional dead dead time can be dead by adjusting the channel *dead_time* configuration parameter. When this is different that zero, the channel will require an additional N clock cycles with *trigger_B* deactive before re-arming.

Refresh

While in the READY state, the voltages stored in the currently selected set of C_X buffers shift slowly due to leakage effects, which affects the time and charge measurements. In order to keep this effect under 0.1 LSB, whenever the channel has been in READY state for 99.2 µs[1], a invalid event is triggered causing the channel to rearm with the next, fresh, set of C_X

5.9 Event counter

TOFPET 2C includes event counting features, which allow events to be counted without being transmitted (and thus, not subject to event conversion and transmission limitation).

The counter feature allows the counting period to be globally set (table 28) and the counting mode to be set on a per-channel basis (table 29).

The count data is transmitted using the same data links as the events.

Table 28: Counter period settings.

counter_en	counter_period	Counting period
0b0	any	Counter disabled
0b1	0x0	2^{10} TDC_CLK cycles.
0b1	0x1	2^{12} TDC_CLK cycles.
0b1	0x2	2^{14} TDC_CLK cycles.
0b1	0x3	2^{16} TDC_CLK cycles.
0b1	0x4	2^{18} TDC_CLK cycles.
0b1	0x5	2^{20} TDC_CLK cycles.
0b1	0x6	2^{22} TDC_CLK cycles.
0b1	0x7	2^{24} TDC_CLK cycles.

[1] 200 MHz TDC_CLK.

Table 29: Channel counting modes.

counter_mode	Counting mode
0x0	Never count. If count_en is 0b1, the transmitted value is always zero.
0x1	Always count. If count_en is 0b1, the transmitted value should be $min\left\{counting\ period, 2^{24}\right\}-1$.
0x2	Count valid events.
0x3	Count invalid events.
0x8	Count all events.
0xC	Count numer of rising edges in trigger_B.
0xF	Count number of cycles during which trigger_B is active.

6 Debug outputs

TOFPET 2C has two sets of debug outputs.

6.1 Channel 63 analog debug outputs

Channel 63's *Vout_T* and *Vth_T*1 are exposed into two analog pins, CH63_VOUT_T and CH63_VOUT_TH1. These can be enabled by setting the global *adebug_out_mode* and $adebug_buffer$ configuration values per table 30.

Table 30: Analog debug outputs

adebug_out_mode	**adebug_buffer**	Analog debug output
0b11	0b1	Disabled.
0b01	0b0	Enabled

With default settings, CH63_VOUT_T should have a baseline of ≈460 mV, while CH63_VOUT_TH1 should have a DC voltage between ≈460 mV and ≈660 mV depending on the settings of threshold T1.

Remarks:

- CH63_VOUT_T must be probed with a very low capacitance circuit (eg, an oscilloscope active probe).
- The signal CH63_VOUT_T may be slower than the actual *Vout_T*.

6.2 Digital analog debug outputs

Table 31: Digital debug outputs

(global) debug_mode	**(channel) debug_mode**	**tx3**	**tx2**	**tx1**
0b0	0b00	Data	Data	Data
0b1	0b00	0	0	0
0b1	0b01	do_T1'	do_T2	do_E
0b1	0b10	trigger_T	trigger_E	trigger_B

Remarks:

- This feature can only be used when TOFPET 2C is configured to transmit data over a single link (tx0).
- Do not enable *debug_mode* on more than a single channel per ASIC.

7 Data transmission

Event and counter data are transmitted over TX[3..0] using 8B/10B coding, as sequence of 8 symbols (80-bit) containing 1 K28.1 symbol and 7 data symbols representing 56-bit of data. K28.5 symbols are transmitted during link idle times.

K28.1 and K28.5 are the only K codes transmitted by TOFPET 2C. This can be used for sthe 0011111xxx and 1100000xxx bit sequences

The link operation mode is configurable, as described in tables 32 and 33:

- 4, 2 or 1 links can be used.
- Links can operate in SDR or DDR mode.

Table 32: Number of active links

tx_nlinks	Links active
0b00	1 (fig. 17)
0b01	2 (fig. 18)
0b10	4 (fig. 19)

Table 33: Link rate mode

tx_ddr	Link mode
0b0	Links operate in SDR mode (1 bit per CLK period).
0b1	Links operate in DDR mode (2 bits per CLK period).

Figure 17: Data transmission with 1 link in DDR mode.

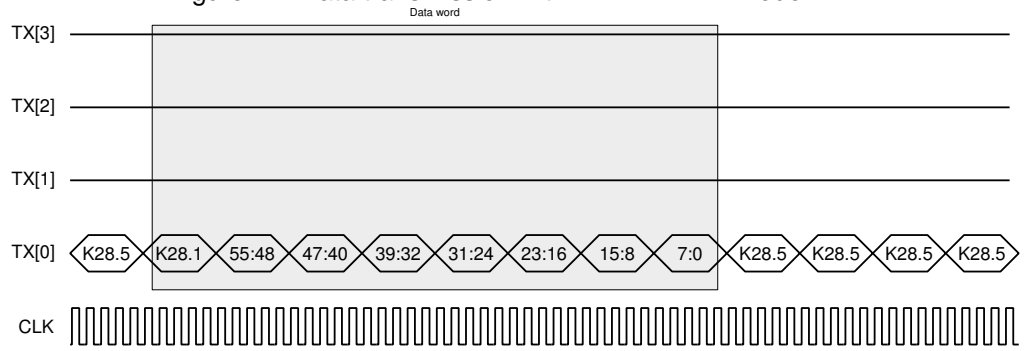
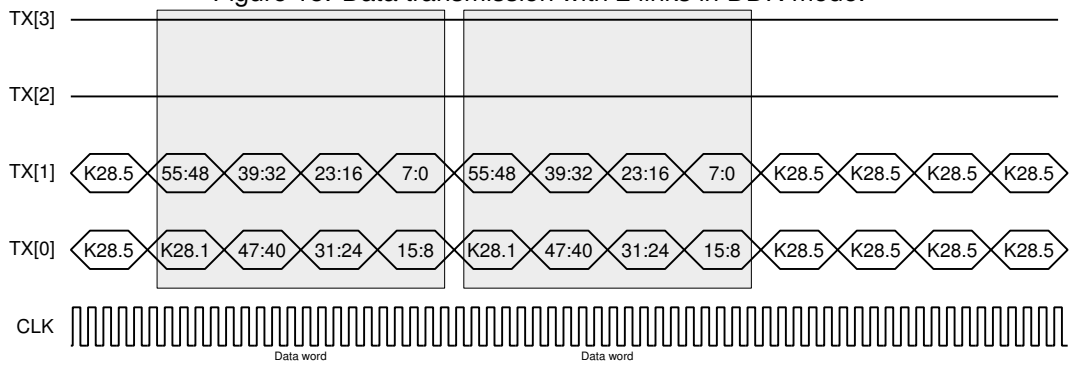


Figure 18: Data transmission with 2 links in DDR mode.



7.1 Link receiver training patterns

In addition to normal data transmission, the data links can also be used to transmit patterns for link receiver training as per table 34.

7.2 Event data words

When a valid event is detected, it is be digitized and transmitted outside, as per table 35.

Figure 19: Data transmission with 4 links in DDR mode.

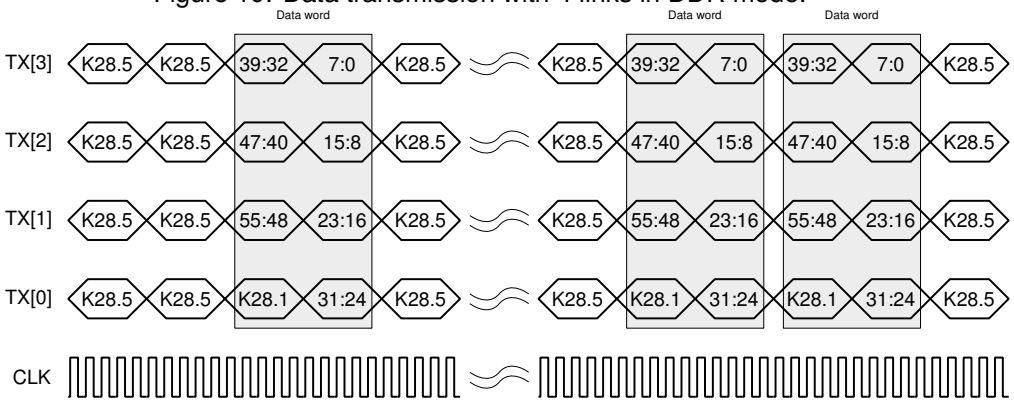


Table 34: Link operation mode

tx_mode	Link operation mode
0b00	Receiver training pattern 0b00: sequences of 0101010101... (fig 20)
0b01	Receiver training pattern 0b01: sequences of 0000011111... (fig 21)
0b10	Normal data transmission.

Figure 20: Data link training pattern 0b00 (4 links selected).

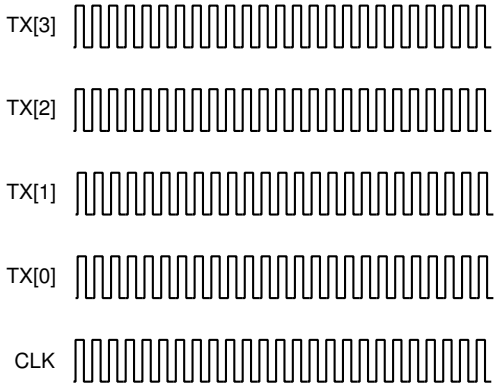
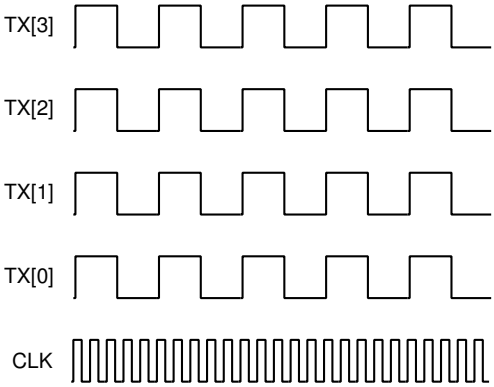


Figure 21: Data link training pattern 0b01 (4 links selected).



- *tcoarse*, *ecoarse* and *qcoarse* are taken from a free running counter and are thus subject to wrap-around.
- The digitization and transmission process takes an average of ≈2 µs but can take up to 20 µs.
- The *tfine′* value which is actually transmitted by TOFPET has a wrap around effect according to equation 5. The same applies for *efine′* and *qfine′*.

$$tfine' = (tfine + 1024 - 14) \bmod 1024 \tag{5}$$

Table 35: Data word content

Bits	Content	Description
55:54	0b10	Word type identifier
53:48	*channel_id*	Input channel index.
47:46	*tac_id*	Internal channel buffer index.
45:30	*tcoarse*	T TDC coarse time tag.
29:20	*e/qcoarse*	E TDC coarse time tag or QDC end of integration time tag.
19:10	*tfine′*	T TDC fine time measurement.
9:0	*e/qfine′*	E TDC fine time measurement or QDC charge measurement.

7.3 Counter data words

Table 36: Count word content

Bits	Content	Description
55:48	0b00000001	Word type identifier
47:30:	Reserved	
29:24	channel_id	Input channel index.
23:0	count	Count value.

7.4 Heartbeat words

If nothing has been transmitted for some time, the ASIC will send a heartbeat word t_{idle} clock cycles after the last word has been sent.

- The transmission may appear periodic but it's actually relative to the last word sent.

Table 37: Heartbeat word content

Bits	Content	Description
55:0	0x000000AABBCCDD	Word type identifier

Table 38: Heartbeat idle delays

Link mode	Links active	t_{idle} (CLK cycles)
SDR	1	81920
	2	40960
	4	20480
DDR	1	40960
	2	20480
	4	10240

8 Typical performance characteristics

$VDD12 = 1.2V$, $VDD25 = 2.5\ V$, $T_A = 18\ °C$

Figure 22: I_{VDD12} versus *fe_ib2*

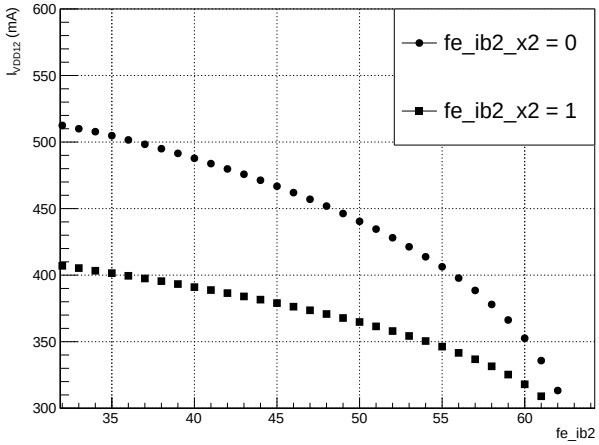


Figure 23: I_{VDD12} versus *disc_sf_bias*

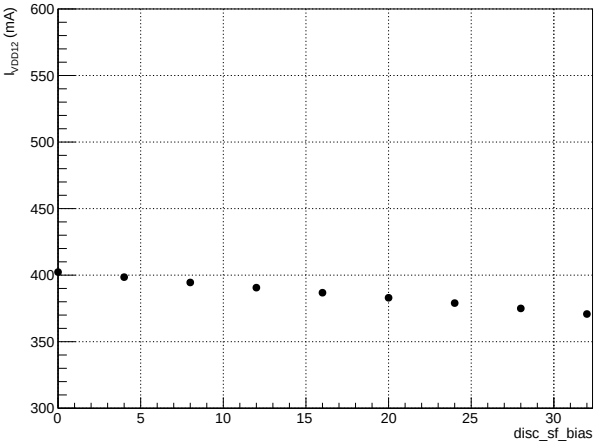


Figure 24: Noise count rate versus threshold (T1).

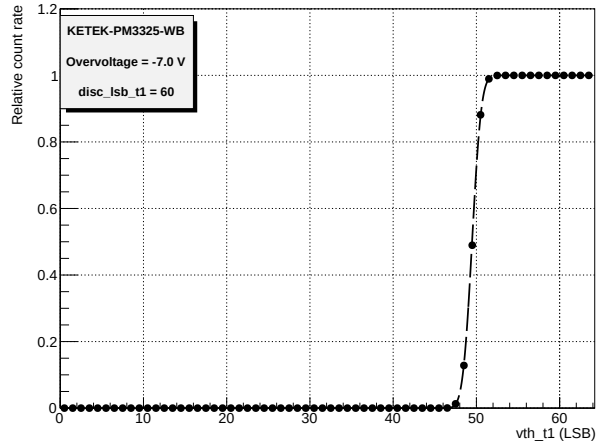


Figure 25: SiPM dark count rate versus threshold (T1).

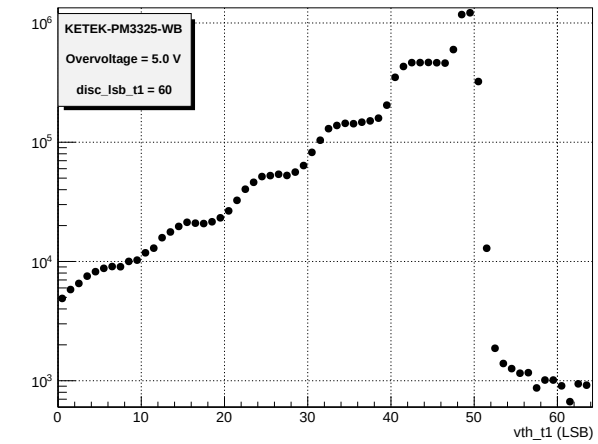


Figure 26: TDC DNL vs. Output Code

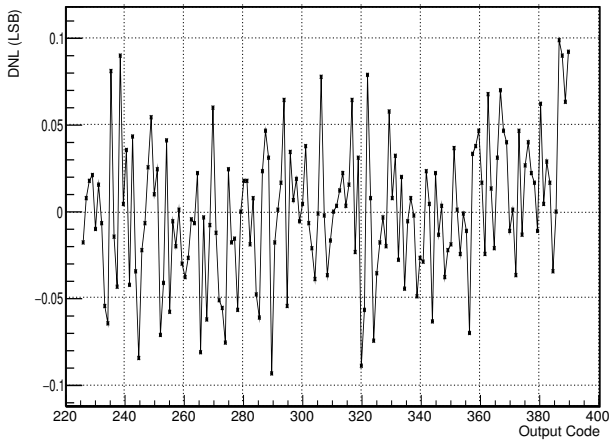


Figure 27: TDC INL vs. Output Code

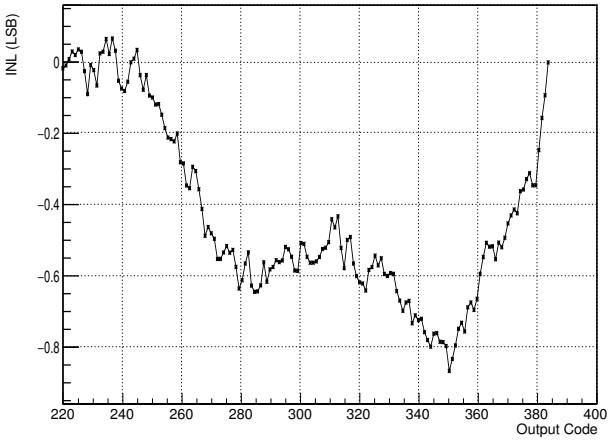


Figure 28: TDC bin distribution

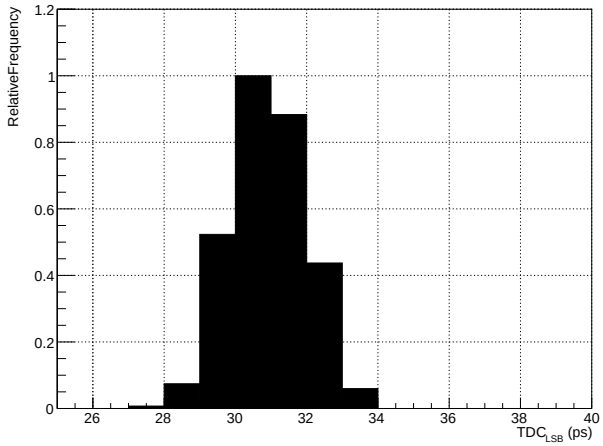


Figure 29: TDC error: 1 vs 64 simultaneous hits

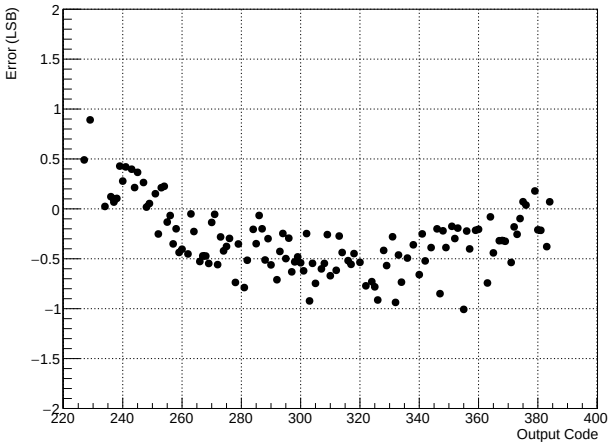


Figure 30: QDC DNL vs. Output Code

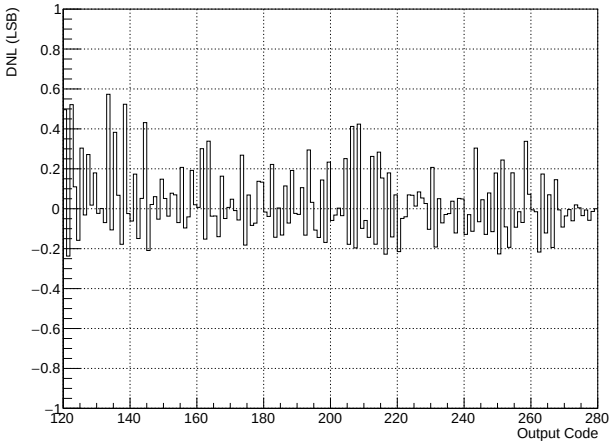


Figure 31: QDC INL vs. Output Code

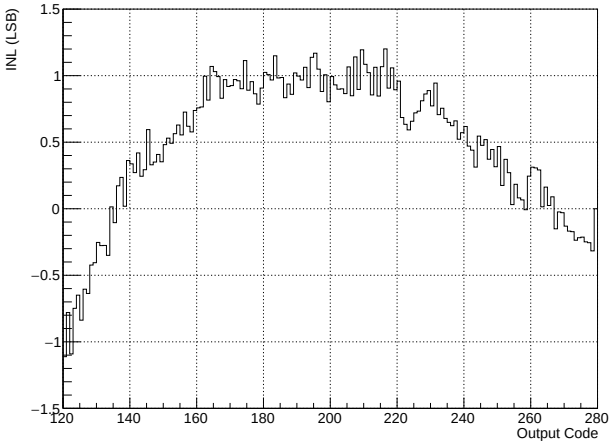


Figure 32: QDC noise

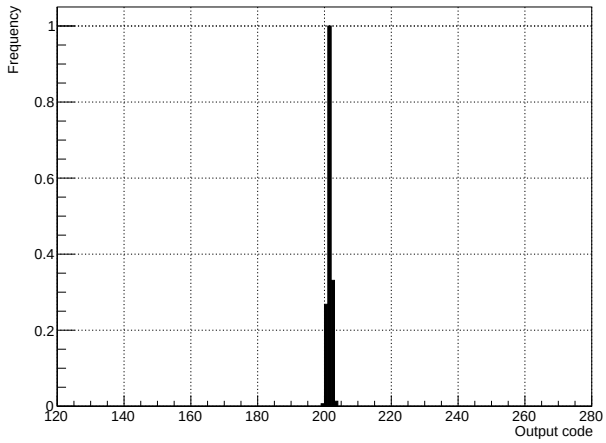


Figure 33: QDC error: 1 vs 64 simultaneous hits

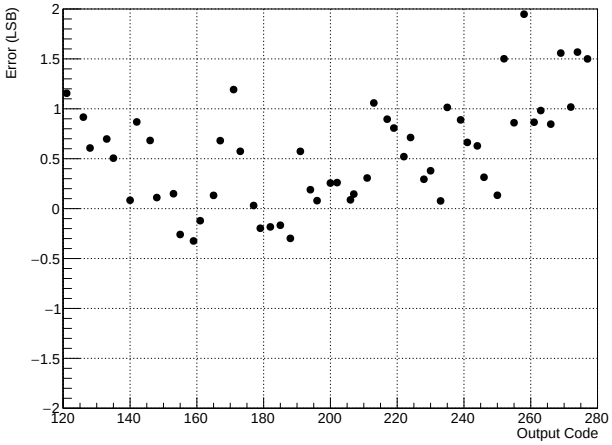


Figure 34: TDC temperature drift

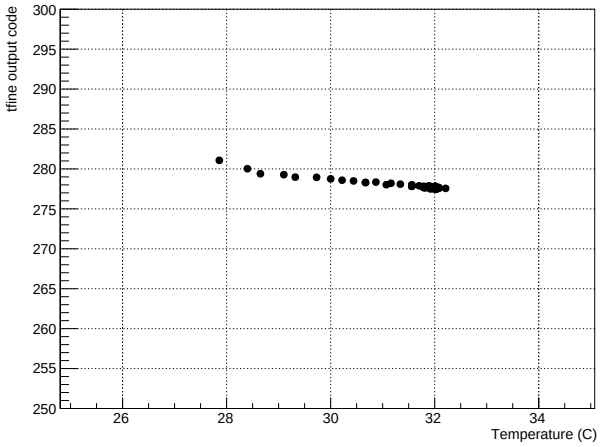
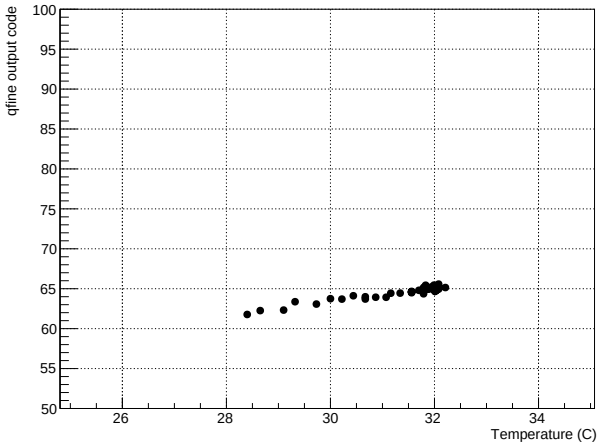


Figure 35: QDC temperature drift



9 Trigger modes

TOFPET 2 implements a variety of configurable trigger modes. The following is a non-exaustive list of possible trigger configurations intended as guide for users.

9.1 Single threshold trigger: T1

This mode is suitable when the both the adequate timing threshold and amplitude discrimination are identical and within the dynamic range of the T branch. In this mode discriminator T1 is used for all purposes and all events which cross vth_T1 are accepted.

Table 39: Single threshold trigger: T1

Setting	Value	Note
disc_lsb_t1	62 .. 55	Application dependent.
fe_delay	OFF	Delay line bypassed.
trigger_mode_2_t	0b00	Time stamp taken on rising edge of *do_T*1.
trigger_mode_2_q	0b00	Integration started on rising edge of *do_T*1.
trigger_mode_2_e	0b000	Validation and second time stamp taken on falling edge of *do_T*1.
trigger_mode_2_b	0b000	Rearm and end of variable window integration taken on fall of *do_T*1.

9.2 Single threshold trigger: E

This mode is suitable when the the adequate timing threshold and amplitude discrimination are identical and within the dynamic range of the E branch. In this mode discriminator E is used for all purposes and all events which cross vth_E are accepted.

Table 40: Single threshold trigger: E

Setting	Value	Note
disc_lsb_e	50	Maximum dynamic range.
fe_delay	OFF	Delay line bypassed.
trigger_mode_2_t	0b11	Time stamp taken on rising edge of *do_E*.
trigger_mode_2_q	0b10	Integration started on rising edge of *do_E*.
trigger_mode_2_e	0b010	Validation and second time stamp taken on falling edge of *do_E*.
trigger_mode_2_b	0b010	Rearm and end of variable window integration taken on fall of *do_E*.

9.3 Dual threshold trigger: T1, T2

This mode is suitable when the adequate timing threshold and amplitude discrimination are not identical but both are within the dynamic range of the T branch. In this mode discriminator T1 is used to take the first timestamp and start the integration while T2 is used for energy validation and second timestamp. All events which cross vth_T1 cause the logic to trigger but only those which cross vth_T2 are digitized and accepted.

Table 41: Dual threshold trigger: T1, T2

Setting	Value	Note
disc_lsb_t1	62 .. 55	Application dependent.
disc_lsb_t2	55	Maximum dynamic range.
fe_delay	OFF	Delay line bypassed.
trigger_mode_2_t	0b00	Time stamp taken on rising edge of *do_T*1.
trigger_mode_2_q	0b00	Integration started on rising edge of *do_T*1.
trigger_mode_2_e	0b001	Validation and second time stamp taken on falling edge of *do_T*2.
trigger_mode_2_b	0b011	Rearm and end of variable window integration taken on fall of *do_T*1 + *do_T*2.

9.4 Dual threshold trigger: T1, E

This mode is suitable when the adequate timing threshold and amplitude discrimination are neither identical nor within the dynamic range of the same branch. In this mode discriminator T1 is used to take the first timestamp and start the integration while E is used for energy validation and second timestamp. All events which cross vth_T1 cause the logic to trigger but only those which cross vth_E are digitized and accepted.

Table 42: Dual threshold trigger: T1, E

Setting	Value	Note
disc_lsb_t1	62 .. 55	Application dependent.
disc_lsb_e	50	Maximum dynamic range.
fe_delay	OFF	Delay line bypassed.
trigger_mode_2_t	0b00	Time stamp taken on rising edge of do_T1.
trigger_mode_2_q	0b00	Integration started on rising edge of do_T1.
trigger_mode_2_e	0b010	Validation and second time stamp taken on falling edge of do_E.
trigger_mode_2_b	0b100	Rearm and end of variable window integration taken on fall of $do\_T1 + do\_E$.

9.5 Dual threshold trigger: T1, T2 with fast dark count rejection

This mode is suitable when the adequate timing threshold and amplitude discrimination are not identical but both are within the dynamic range of the T branch and fast rejection of dark counts is required. In this mode discriminator T1 is used to take the first timestamp while T2 is used to start the integration, energy validation and second timestamp. Events which cross vth_T1 but not not vth_T2 are rejected withotu any logic deat time. Events which cross vth_T2 are digitized and accepted.

Table 43: Dual threshold trigger: T1, T2

Setting	Value	Note
disc_lsb_t1	62 .. 55	Application dependent.
disc_lsb_t2	55	Maximum dynamic range.
fe_delay	3-8 ns	Application dependent.
trigger_mode_2_t	0b01	Time stamp taken on rising edge of $do\_T1' \cdot do\_T2$.
trigger_mode_2_q	0b01	Integration started on rising edge of do_T2.
trigger_mode_2_e	0b001	Validation and second time stamp taken on falling edge of do_T2.
trigger_mode_2_b	0b011	Rearm and end of variable window integration taken on fall of $do\_T1 + do\_T2$.

9.6 Tripple threshold trigger: T1, T2, E with fast dark count rejection

This mode is suitable when the adequate timing threshold and amplitude discrimination are neither identical nor within the dynamic range of the same branch and fast dark coutn rejection is required. In this mode discriminator T1 is used to take the first timestamp while T2 is used to start the integration and E is used for energy validation and second timestamp. Events which cross vth_T1 but not not vth_T2 are rejected withotu any logic deat time. Events which cross vth_T2 cause the logic to trigger but ony those which cross vth_E are digitized and accepted.

Table 44: Dual threshold trigger: T1, T2

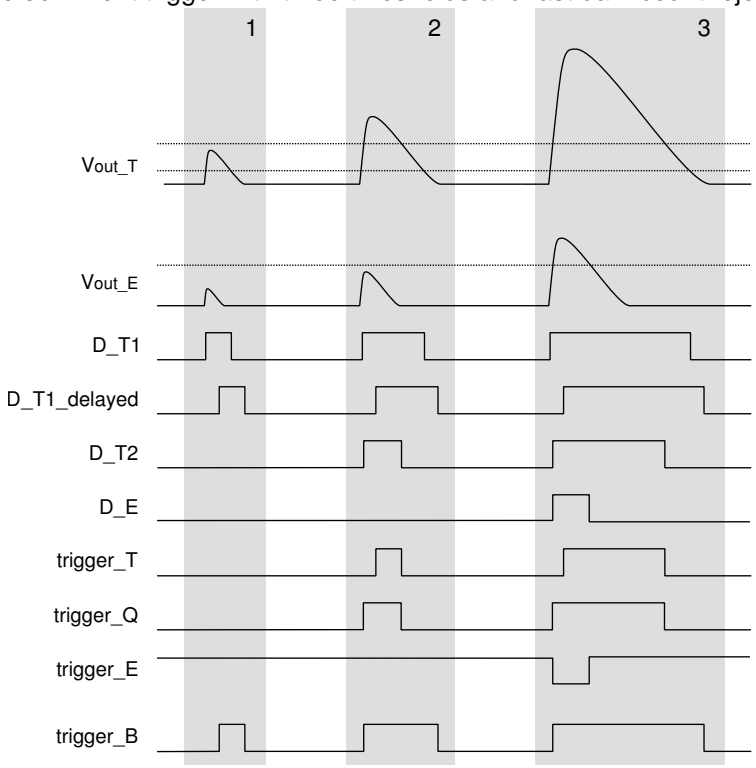
Setting	Value	Note
disc_lsb_t1	62 .. 55	Application dependent.
disc_lsb_t2	55	Maximum dynamic range.
disc_lsb_e	50	Maximum dynamic range.
fe_delay	3-8 ns	Application dependent.
trigger_mode_2_t	0b01	Time stamp taken on rising edge of $do\_T1' \cdot do\_T2$.
trigger_mode_2_q	0b01	Integration started on rising edge of do_T2.
trigger_mode_2_e	0b010	Validation and second time stamp taken on falling edge of do_E.
trigger_mode_2_b	0b101	Rearm and end of variable window integration taken on fall of $do\_T1 + do\_T2 + do\_E$.

Figure 36 illustrates the operation in the 3 cases.

- Event 1 triggers only D_T1. It produces no rising edges on trigger_T, trigger_E nor trigger_Q and thus it's totally ignored by the trigger logic.
- Event 2 triggers D_T1 and D_D2, yielding rising edges on trigger_T and trigger_Q. However since there is no rising edge on trigger_E, after the falling edge of trigger_B the logic will discard the event and then REARM for the text event.
- Event 3 triggers all 3 discriminator, yielding riding edges on all 4 trigger signals. After the falling edge of trigger_B the logic will queue the event for digitization and transmission and and then REARM for the next event.

Note that due to DELAY, the time of the rising edge of trigger_T is actually the time of the rising edge of D_T1 + DELAY, not the time of the rising edge of D_T2.

Figure 36: Event trigger with three thresholds and fast dark count rejection.



10 Calibration

This section describes the calibration methods currently recommended by PETsys and implemented in the PETsys software.

10.1 TIA baseline and discriminators

The purpose of this procedure is to

- Adjust the TIA output baseline such that it is in the range of the threshold voltage DAC.
- Determine which setting of threshold voltage DAC corresponds to the TIA output baseline.
- Estimate the noise in the TIA and discriminator.

It is described for discriminator T1 but the process for discriminator T2 and E is identical.
This procedure should be done with the sensors connected, but biased in such a way they produce no signal. Eg, SiPM should be biased below their breakdown voltage.

10.1.1 Baseline adjustment

1. Set *count_mode* to 0xF.
2. Set *count_en* to 0b1 and set *counter_period*.
3. Set *trigger_2_b* to select the desired discriminator.
4. Set threshold voltage *vth_T*1 to 62.
5. Set *baseline_T* to 62.
6. Increase *baseline_T* until the baseline is above the threshold voltage.
   (a) Read the counter.
   (b) If the counter is less than 99.9% of maximum, then increase *baseline_T* by one and repeat.
7. Use this value of *baseline_T* in all further data acquisitions.

10.1.2 Threshold calibration

1. Set *count_mode* to 0xF.
2. Set *count_en* to 0b1 and set *counter_period*.
3. Set *trigger_2_b* to select the desired discriminator.
4. Iterate setting threshold voltage *vth_T*1 in 63 to 0.
   (a) Read the counter.
   (b) Store the counter value.

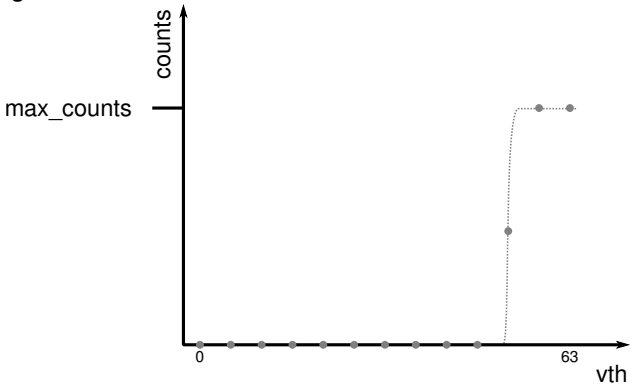
The collected data is a S-curve (figure 37). Fitting the cumulating distribution function to the data, μ gives the position of the baseline in terms of the threshold voltage, while σ provides an estimate of noise.

10.1.3 Dark counts

The internal counter can also be used mesure the dark count rate of the SiPM in function of threshold. The same method is used as in 10.1.2 but

- SiPM should be biased at the desired operation voltage.
- *count_mode* should be set to 0xC.

Figure 37: Discriminator counts as function of threshold.



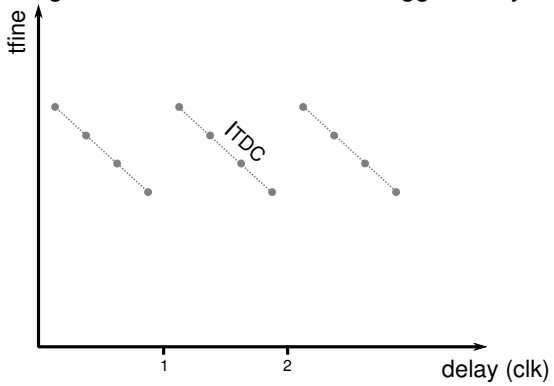
10.2 TDC calibration

The purpose of this procedure is to characterize the response of the TDC as function of the trigger signal phase relative to the clock, in order to obtain a correction curve. This method uses an external TEST_PULSE signal, synchronous to the clock but adjustable phase/delay in order to scan the phase of the trigger signal.

1. Set measurement mode to ToT (see 5.5).
2. Set *trigger_mode*_1 to 0b01.
3. For a range of delays (eg, 0 to 40 ns in 100 ps increments):
   (a) Transmit to the TEST_PULSE input pulses with a synchronous relationship to *CLK* but with the chosen delay.
   (b) Collect data.

The collected data (figure 38)can be fitted to a function (eg, a 2nd order polynomial) in order to extract the correction curve.

Figure 38: tfine as function of trigger delay.



10.3 QDC calibration

The purpose of this procedure is to characterize the response of the QDC response as function of the integration time and integrated charge. This method uses an external TEST_PULSE signal, synchronous to the clock but adjustable phase/delay and length to scan the integration window duration.

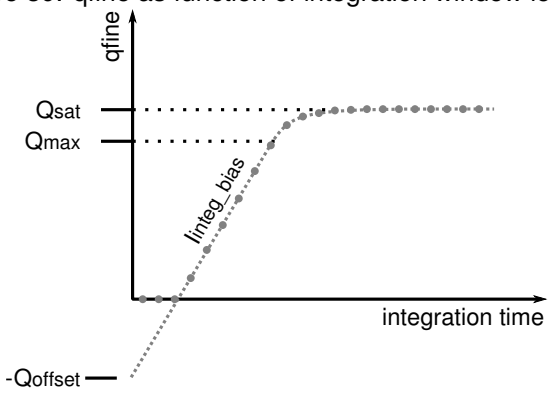
This procedure should be done with the sensors connected, but biased in such a way they produce no signal. Eg, SiPM should be biased below their breakdown voltage.

1. Set measurement mode to QDC (see 5.5).
2. Set *trigger_mode*_1 to 0b01.
3. Set *min_intg_time* to 0 and *max_intg_time* to 127.

4. For a range of lengths (eg, 0 to 500 ns) and delays (0 to 5.0 ns in 250 ps increments):
   (a) Transmit to the TEST_PULSE input test pulses with a synchronous relationship to *CLK* but with the chosen length and delay.
   (b) Collect data.

The collected data (figure 38)can be fitted to a function in order to extract the correction curve.

Figure 39: qfine as function of integration window length.



11 Package and pin description

11.1 Pin description

Pin	Pin name	Pin type	Description
K1	CH_00	Analog IN	Channel 00
K2	CH_01	Analog IN	Channel 01
J1	CH_02	Analog IN	Channel 02
J2	CH_03	Analog IN	Channel 03
H1	CH_04	Analog IN	Channel 04
H2	CH_05	Analog IN	Channel 05
G1	CH_06	Analog IN	Channel 06
G2	CH_07	Analog IN	Channel 07
F1	CH_08	Analog IN	Channel 08
F2	CH_09	Analog IN	Channel 09
E1	CH_10	Analog IN	Channel 10
E2	CH_11	Analog IN	Channel 11
D1	CH_12	Analog IN	Channel 12
D2	CH_13	Analog IN	Channel 13
C1	CH_14	Analog IN	Channel 14
C2	CH_15	Analog IN	Channel 15
B1	CH_16	Analog IN	Channel 16
B2	CH_17	Analog IN	Channel 17
A1	CH_18	Analog IN	Channel 18
A2	CH_19	Analog IN	Channel 19
A3	CH_20	Analog IN	Channel 20
B3	CH_21	Analog IN	Channel 21
A4	CH_22	Analog IN	Channel 22
B4	CH_23	Analog IN	Channel 23
A5	CH_24	Analog IN	Channel 24
B5	CH_25	Analog IN	Channel 25
B6	CH_26	Analog IN	Channel 26
A7	CH_27	Analog IN	Channel 27
B7	CH_28	Analog IN	Channel 28
A8	CH_29	Analog IN	Channel 29
B8	CH_30	Analog IN	Channel 30
A9	CH_31	Analog IN	Channel 31
B9	CH_32	Analog IN	Channel 32
A10	CH_33	Analog IN	Channel 33
B10	CH_34	Analog IN	Channel 34
A11	CH_35	Analog IN	Channel 35
B11	CH_36	Analog IN	Channel 36
B12	CH_37	Analog IN	Channel 37
A13	CH_38	Analog IN	Channel 38
B13	CH_39	Analog IN	Channel 39
A14	CH_40	Analog IN	Channel 40
B14	CH_41	Analog IN	Channel 41
A15	CH_42	Analog IN	Channel 42
B15	CH_43	Analog IN	Channel 43
A16	CH_44	Analog IN	Channel 44
A17	CH_45	Analog IN	Channel 45
B16	CH_46	Analog IN	Channel 46
B17	CH_47	Analog IN	Channel 47
C16	CH_48	Analog IN	Channel 48
C17	CH_49	Analog IN	Channel 49
D16	CH_50	Analog IN	Channel 50
D17	CH_51	Analog IN	Channel 51
E16	CH_52	Analog IN	Channel 52
E17	CH_53	Analog IN	Channel 53
F16	CH_54	Analog IN	Channel 54

F17	CH_55	Analog IN	Channel 55
G16	CH_56	Analog IN	Channel 56
G17	CH_57	Analog IN	Channel 57
H16	CH_58	Analog IN	Channel 58
H17	CH_59	Analog IN	Channel 59
J16	CH_60	Analog IN	Channel 60
J17	CH_61	Analog IN	Channel 61
K16	CH_62	Analog IN	Channel 62
K17	CH_63	Analog IN	Channel 63
N17	CH_63_VOUT_TH1	Analog OUT	Channel 63 Vth_T1
M17	CH_63_VOUT_T	Analog OUT	Channel 63 Vout_T
A6	AGND	GND	Analog ground
A12	AGND	GND	Analog ground
C3	AGND	GND	Analog ground
C4	AGND	GND	Analog ground
C6	AGND	GND	Analog ground
C8	AGND	GND	Analog ground
C9	AGND	GND	Analog ground
C10	AGND	GND	Analog ground
C12	AGND	GND	Analog ground
C14	AGND	GND	Analog ground
C15	AGND	GND	Analog ground
E4	AGND	GND	Analog ground
E14	AGND	GND	Analog ground
F6	AGND	GND	Analog ground
F7	AGND	GND	Analog ground
F8	AGND	GND	Analog ground
F9	AGND	GND	Analog ground
F10	AGND	GND	Analog ground
F11	AGND	GND	Analog ground
F12	AGND	GND	Analog ground
G6	AGND	GND	Analog ground
G7	AGND	GND	Analog ground
G8	AGND	GND	Analog ground
G9	AGND	GND	Analog ground
G10	AGND	GND	Analog ground
G11	AGND	GND	Analog ground
G12	AGND	GND	Analog ground
H3	AGND	GND	Analog ground
H6	AGND	GND	Analog ground
H7	AGND	GND	Analog ground
H8	AGND	GND	Analog ground
H9	AGND	GND	Analog ground
H10	AGND	GND	Analog ground
H11	AGND	GND	Analog ground
H12	AGND	GND	Analog ground
H15	AGND	GND	Analog ground
J6	AGND	GND	Analog ground
J7	AGND	GND	Analog ground
J8	AGND	GND	Analog ground
J9	AGND	GND	Analog ground
J10	AGND	GND	Analog ground
J11	AGND	GND	Analog ground
J12	AGND	GND	Analog ground
K6	AGND	GND	Analog ground
K7	AGND	GND	Analog ground
K8	AGND	GND	Analog ground
K9	AGND	GND	Analog ground
K10	AGND	GND	Analog ground
K11	AGND	GND	Analog ground

K12	AGND	GND	Analog ground
L1	AGND	GND	Analog ground
L2	AGND	GND	Analog ground
L4	AGND	GND	Analog ground
L14	AGND	GND	Analog ground
L16	AGND	GND	Analog ground
L17	AGND	GND	Analog ground
L3	AIOGND_B	GND	Analog ground
L15	AIOGND_T	GND	Analog ground
L6	DGND	GND	Digital ground
L7	DGND	GND	Digital ground
L8	DGND	GND	Digital ground
L9	DGND	GND	Digital ground
L10	DGND	GND	Digital ground
L11	DGND	GND	Digital ground
L12	DGND	GND	Digital ground
M2	DGND	GND	Digital ground
M3	DGND	GND	Digital ground
M6	DGND	GND	Digital ground
M7	DGND	GND	Digital ground
M8	DGND	GND	Digital ground
M9	DGND	GND	Digital ground
M10	DGND	GND	Digital ground
M11	DGND	GND	Digital ground
M12	DGND	GND	Digital ground
M15	DGND	GND	Digital ground
M16	DGND	GND	Digital ground
P1	DGND	GND	Digital ground
P17	DGND	GND	Digital ground
R1	DGND	GND	Digital ground
R2	DGND	GND	Digital ground
R3	DGND	GND	Digital ground
R4	DGND	GND	Digital ground
R5	DGND	GND	Digital ground
R6	DGND	GND	Digital ground
R7	DGND	GND	Digital ground
R8	DGND	GND	Digital ground
R9	DGND	GND	Digital ground
R10	DGND	GND	Digital ground
R11	DGND	GND	Digital ground
R12	DGND	GND	Digital ground
R13	DGND	GND	Digital ground
R14	DGND	GND	Digital ground
R15	DGND	GND	Digital ground
R16	DGND	GND	Digital ground
R17	DGND	GND	Digital ground
T1	DGND	GND	Digital ground
T6	DGND	GND	Digital ground
T7	DGND	GND	Digital ground
T11	DGND	GND	Digital ground
T12	DGND	GND	Digital ground
T17	DGND	GND	Digital ground
U1	DGND	GND	Digital ground
U6	DGND	GND	Digital ground
U7	DGND	GND	Digital ground
U11	DGND	GND	Digital ground
U12	DGND	GND	Digital ground
U17	DGND	GND	Digital ground
N2	IOGND_B	GND	Digital ground
N16	IOGND_T	GND	Digital ground

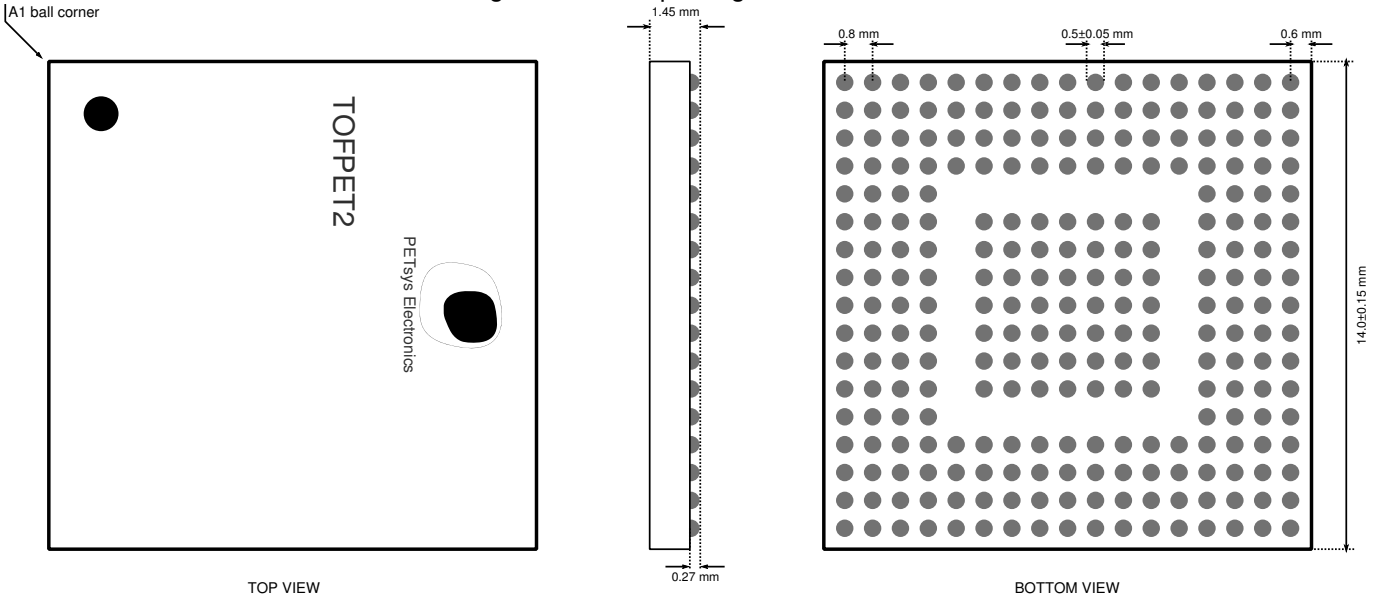
U9	CLK_N	LVDS IN	CLK
T9	CLK_P	LVDS IN	CLK
U13	MOSI_N	LVDS IN	MOSI
T13	MOSI_P	LVDS IN	MOSI
U15	SCLK_N	LVDS IN	SCLK
T15	SCLK_P	LVDS IN	SCLK
U10	SS_N	LVDS IN	SS
T10	SS_P	LVDS IN	SS
U8	SYNC_RST_N	LVDS IN	SYNC_RST
T8	SYNC_RST_P	LVDS IN	SYNC_RST
U16	TEST_PULSE_N	LVDS IN	TEST_PULSE
T16	TEST_PULSE_P	LVDS IN	TEST_PULSE
U14	MISO_N	LVDS OUT	MISO
T14	MISO_P	LVDS OUT	MISO
U5	TX0_N	LVDS OUT	TX[0]
T5	TX0_P	LVDS OUT	TX[0]
U4	TX1_N	LVDS OUT	TX[1]
T4	TX1_P	LVDS OUT	TX[1]
U3	TX2_N	LVDS OUT	TX[2]
T3	TX2_P	LVDS OUT	TX[2]
U2	TX3_N	LVDS OUT	TX[3]
T2	TX3_P	LVDS OUT	TX[3]
C5	N/C	N/C	Not connected
C7	N/C	N/C	Not connected
C11	N/C	N/C	Not connected
C13	N/C	N/C	Not connected
D3	N/C	N/C	Not connected
D4	N/C	N/C	Not connected
D9	N/C	N/C	Not connected
D14	N/C	N/C	Not connected
D15	N/C	N/C	Not connected
F3	N/C	N/C	Not connected
G3	N/C	N/C	Not connected
G15	N/C	N/C	Not connected
K3	N/C	N/C	Not connected
K15	N/C	N/C	Not connected
M1	N/C	N/C	Not connected
N1	N/C	N/C	Not connected
N3	N/C	N/C	Not connected
N15	N/C	N/C	Not connected
P2	N/C	N/C	Not connected
P16	N/C	N/C	Not connected
J3	AIOVDD_B	VDD12	Analog supply
J15	AIOVDD_T	VDD12	Analog supply
D5	AVDD	VDD12	Analog supply
D6	AVDD	VDD12	Analog supply
D7	AVDD	VDD12	Analog supply
D8	AVDD	VDD12	Analog supply
D10	AVDD	VDD12	Analog supply
D11	AVDD	VDD12	Analog supply
D12	AVDD	VDD12	Analog supply
D13	AVDD	VDD12	Analog supply
F14	AVDD	VDD12	Analog supply
G4	AVDD	VDD12	Analog supply
G14	AVDD	VDD12	Analog supply
H4	AVDD	VDD12	Analog supply
J4	AVDD	VDD12	Analog supply
J14	AVDD	VDD12	Analog supply
K4	AVDD	VDD12	Analog supply
K14	AVDD	VDD12	Analog supply

F4	AVDD	VDD12	Analog ground
H14	AVDD	VDD12	Analog ground
M14	DVDD	VDD12	Digital supply
P3	DVDD	VDD12	Digital supply
P4	DVDD	VDD12	Digital supply
P5	DVDD	VDD12	Digital supply
P6	DVDD	VDD12	Digital supply
P7	DVDD	VDD12	Digital supply
P8	DVDD	VDD12	Digital supply
P9	DVDD	VDD12	Digital supply
P10	DVDD	VDD12	Digital supply
P11	DVDD	VDD12	Digital supply
P12	DVDD	VDD12	Digital supply
P13	DVDD	VDD12	Digital supply
P14	DVDD	VDD12	Digital supply
P15	DVDD	VDD12	Digital supply
M4	DVDD	VDD12	Digital supply
N4	IOVDD_B	VDD25	Digital supply
N14	IOVDD_T	VDD25	Digital supply
F15	VG_T	VG	Reference voltage
E3	VREF_B	VREF	Reference voltage
E15	VREF_T	VREF	Reference voltage

Table 45: Pin functional description

11.2 Package outline

Figure 40: BGA package dimensions



11.3 Recommended footprint

Figure 41: BGA footprint

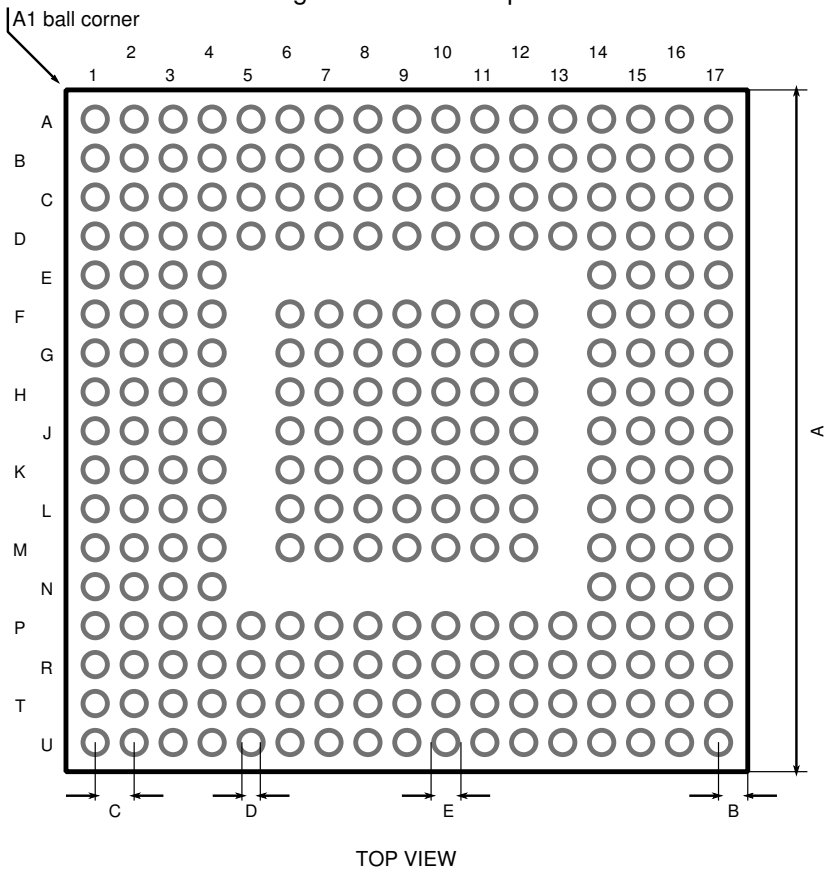


Table 46: BGA foot print recommended sizes

	Description	Value
A	Footprint edge length	14 mm
B	Pad centre to edge distance	0.6 mm
C	Pad centre to centre distance (pitch)	0.8 mm
D	Pad diameter	450 µm
E	Solder mask opening diameter	600 µm

PETsys recommends the use of Non-Solder Mask Defined pads, with dimensions as per figure 41 and table 46.

A CRC-8 example

A possible VHDL implementation would be:

```
function crc8(crc_in : std_logic_vector(7 downto 0); data : std_logic)
        return std_logic_vector is
variable crc_out : std_logic_vector(7 downto 0);
begin
  crc_out(0) := data xor crc_in(7);
  crc_out(1) := data xor crc_in(0) xor crc_in(7);
  crc_out(2) := data xor crc_in(1) xor crc_in(7);
  crc_out(3) := crc_in(2);
  crc_out(4) := crc_in(3);
  crc_out(5) := crc_in(4);
  crc_out(6) := crc_in(5);
  crc_out(7) := crc_in(6);
  return crc_out;
end crc8;
```

The initial value of `crc_in` is 0x80. The expect output for a global register read command (`1001`) is `10100111` and the complete command to be sent to the ASIC is `100110100111`.